1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

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REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0001395489	ENGINEERING RELEASED	2012-03-13

SCHEM,MLB,J30

03/12/12

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16	18	PCH SATA/PCIe/CLK/LPC/SPI	J31_MLB	06/13/2011
17	19	PCH DMI/FDI/PM/Graphics	J31_MLB	06/13/2011
18	20	PCH PCI/USB/TP/RSVD	J31_MLB	06/13/2011
19	21	PCH GPIO/MISC/NCTF	J31_MLB	06/13/2011
20	22	PCH POWER	J31_MLB	06/13/2011
21	23	PCH GROUNDS	J31_MLB	06/13/2011
22	24	PCH DECOUPLING	K90I_MLB	02/15/2011
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24	26	Chipset Support	K90I_MLB	02/15/2011
25	27	USB HUB & MUX	LINDA_J30	09/19/2011
26	28	CPU Memory S3 Support	K90I_MLB	02/15/2011
27	29	DDR3 SO-DIMM Connector A	K90I_MLB	02/15/2011
28	30	DDR3 Byte/Bit Swaps	K90I_MLB	02/15/2011
29	31	DDR3 SO-DIMM Connector B	K90I_MLB	02/15/2011
30	33	SD Card Connector	YONAS_J30	11/03/2011
31	34	DDR3/FRAMEBUF VREF MARGINING	J31_MLB	06/13/2011
32	35	X19/ALS/CAMERA CONNECTOR	K90I_MLB	02/15/2011
33	36	T29 Host (1 of 2)	K90I_MLB	02/15/2011
34	37	T29 Host (2 of 2)	K90I_MLB	02/15/2011
35	38	T29 Power Support	K90I_MLB	02/15/2011
36	39	ETHERNET PHY (CAESAR IV)	J31_MLB	06/15/2011
37	40	Ethernet Connector	K90I_MLB	02/15/2011
38	41	FireWire LLC/PHY (FW643E)	K90I_MLB	02/15/2011
39	42	FireWire Port & PHY Power	K90I_MLB	06/23/2011
40	43	FireWire Connector	K90I_MLB	02/15/2011
41	45	SATA/IR/SIL Connectors	YONAS_J30	11/08/2011
42	46	External A USB3 Connector	J31_MLB	07/08/2011
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44	48	Front Flex Support	K90I_MLB	02/15/2011
45	49	SMC	YONAS_J30	12/21/2011
46	50	SMC Support	YONAS_J30	01/02/2012
47	51	LPC+SPI Debug Connector	J31_MLB	06/15/2011
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50	54	Power Sensors: High Side	YONAS_J30	11/03/2011
51	55	Thermal Sensors	YONAS_J30	08/01/2011
52	56	Fan	K90I_MLB	02/15/2011
53	57	WELLSPRING 1	J31_MLB	07/01/2011
54	58	WELLSPRING 2	JACK_J30	09/28/2011
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56	61	SPI ROM	K90I_MLB	02/15/2011
57	62	AUDIO: CODEC/REGULATOR	KAVITHA_J30	07/25/2011
58	64	AUDIO: DETECT/MIC BIAS	DIRK_J30	02/16/2012
59	65	AUDIO: HEADPHONE FILTER	KAVITHA_J30	07/25/2011
60	66	AUDI0: SPEAKER AMP	KAVITHA_J30	07/25/2011
61	67	AUDIO: JACK	DIRK_J30	11/10/2011
62	68	AUDIO:Jack Translators	DIRK_J30	02/20/2012
63	69	DC-In & Battery Connectors	JACK_J30	07/29/2011
64	70	PBus Supply & Battery Charger	JACK_J30	09/27/2011
65	71	System Agent Supply	JACK_J30	09/28/2011
66	72	5V/3.3V SUPPLY	JACK_J30	08/22/2011
67	73	1.5V DDR3 Supply	JACK_J30	07/28/2011
68	74	CPU IMVP7 & AXG VCore Regulator	JACK_J30	08/03/2011
69	75	CPU IMVP7 & AXG VCore Output	JACK_J30	07/28/2011
70	76	CPUVCCIO (1.05V) Power Supply	JACK_J30	09/28/2011
71	77	Misc Power Supplies	JACK_J30	07/28/2011
72	78	Power FETs	K90I_MLB	02/15/2011
73	79	Power Control 1/ENABLE	K90I_MLB	02/15/2011
74	90	LVDS CONNECTOR	K90I_MLB	02/15/2011
75	93	DisplayPort/T29 A MUXing	K90I_MLB	02/15/2011
76	94	Thunderbolt Connector A	K90I_MLB	02/15/2011
77	97	LCD Backlight Driver	J31_MLB	07/08/2011
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79	101	Memory Constraints	K90I_MLB	02/15/2011
80	102	PCH Constraints 1	K90I_MLB	02/15/2011
81	103	PCH Constraints 2	K90I_MLB	02/15/2011
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83	105	T29 Constraints	K90I_MLB	02/15/2011
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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9058	1	SCHEM,MLB,J30	SCH	CRITICAL	
820-3115	1	PCBF,MLB,J30	PCB	CRITICAL	

DRAWING
TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Tue Mar 13 14:00:17 2012

DRAWING TITLE: SCHEM,MLB,J30

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DRAWING NUMBER: 051-9058 SIZE: D
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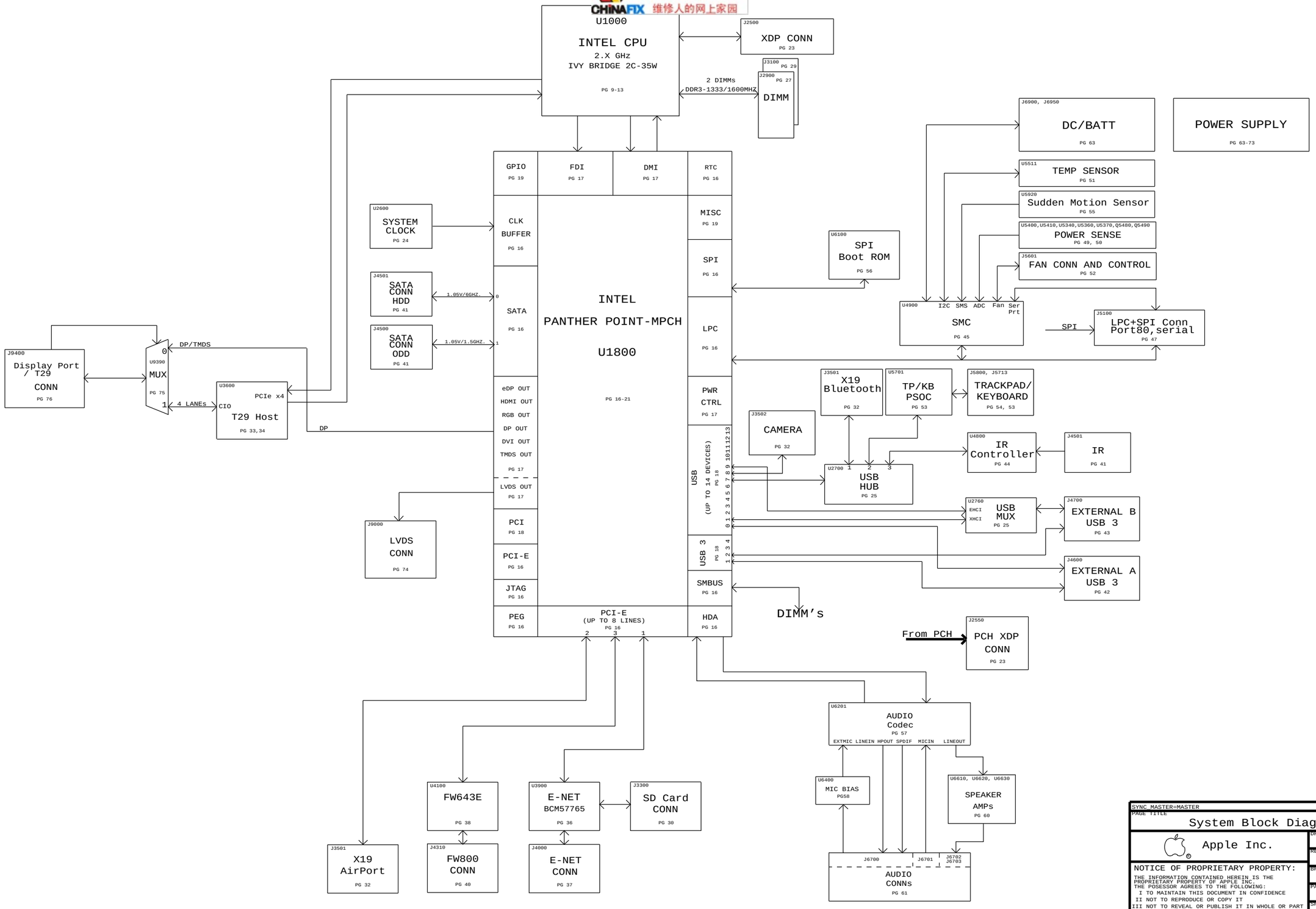

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System Block Diagram

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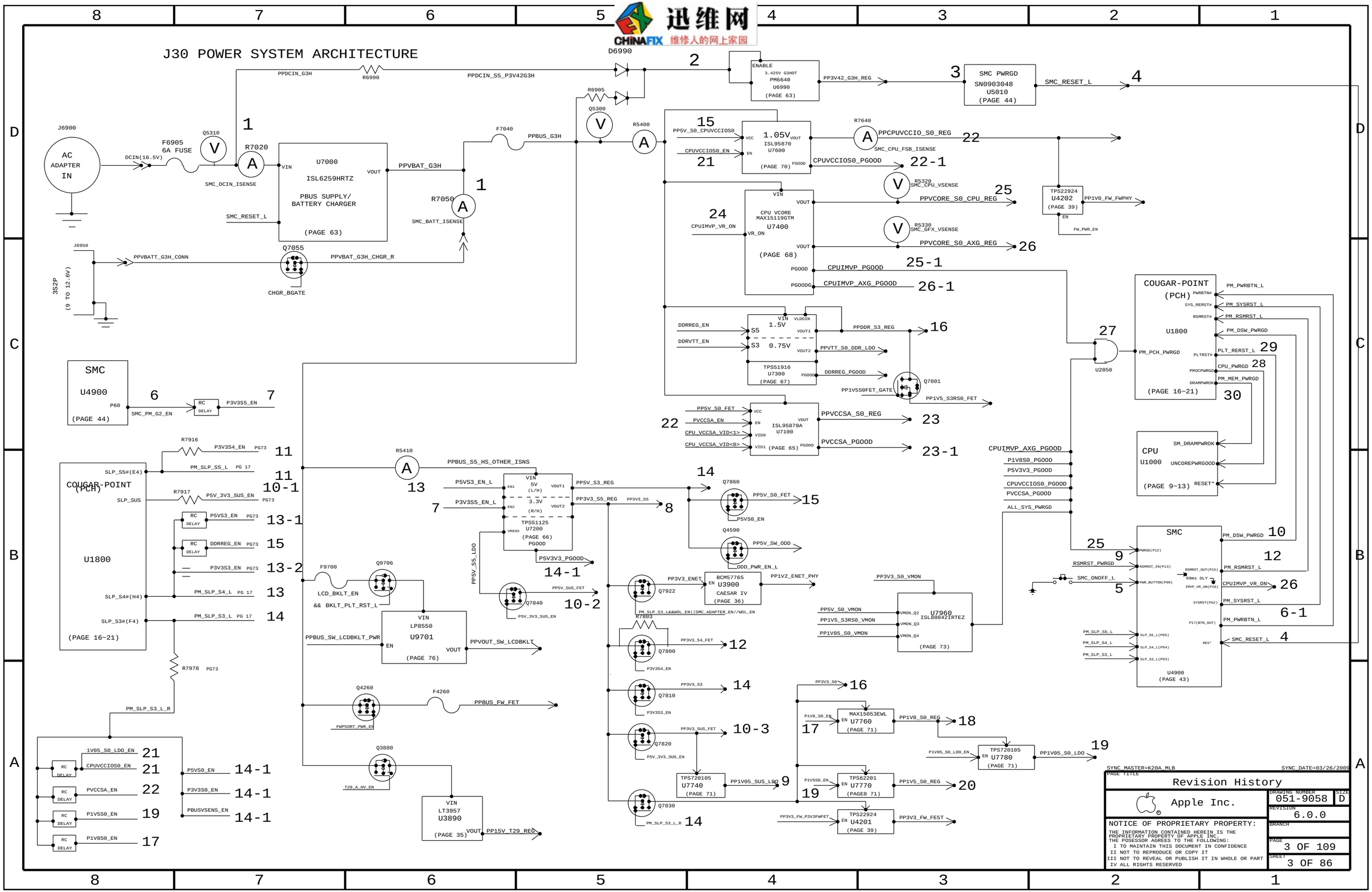
J30 POWER SYSTEM ARCHITECTURE



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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
607-8895	CMN PTS,PCBA,MLB,J30	J30_COMMON,FET_PAIR
085-3092	J30 MLB DEVELOPMENT BOM	J30_DEVEL:ENG
607-8721	POWER FETS PAIR,FAIRCHILD,DDR,J30	DDR_POWER_FET:FAIR
607-8722	POWER FETS PAIR,FAIRCHILD,5V_S3,J30	5V_S3_POWER_FET:FAIR
607-8723	POWER FETS PAIR,FAIRCHILD,PBUS_CHARGER,J30	CHARGER_POWER_FET:FAIR
607-9309	POWER FETS PAIR,RENESAS,DDR,J30	DDR_POWER_FET:REN
607-9310	POWER FETS PAIR,RENESAS,5V_S3,J30	5V_S3_POWER_FET:REN
607-9311	POWER FETS PAIR,RENESAS,PBUS_CHARGER,J30	CHARGER_POWER_FET:REN
639-3752	PCBA,MLB,MOL,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:MOLEX,EEEE_F1YK
639-3756	PCBA,MLB,HYB,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:HYBRID,EEEE_F1YH
639-3753	PCBA,MLB,FOX,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:FOXCONN,EEEE_F1YL
639-3755	PCBA,MLB,HYB,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:HYBRID,EEEE_F1YJ
639-3751	PCBA,MLB,MOL,2.5G,J30	J30_CMNPTS,CPU_2_5GHZ,SODIMM:MOLEX,EEEE_F1YM
639-3754	PCBA,MLB,FOX,2.9G,J30	J30_CMNPTS,CPU_2_9GHZ,SODIMM:FOXCONN,EEEE_F1YG

J30 BOM GROUPS

BOM GROUP	BOM OPTIONS
J30_COMMON	ALTERNATE,COMMON,J30_COMMON1,J30_COMMON2,J30_DEBUG:ENG,J30_PROGPARTS,T29BST:Y,TBTHV:P15V
J30_COMMON1	BATT_3S,CPUMEM_S0,USBHUB2513B,HUB_3NONREM,T29:YES,SDRV_PD,SDRVI2C:MCU,AXG_PHASE1,BTPWR:S4,UV_GLUE_J30
J30_COMMON2	MIKEY,TPAD:Z2,RAMCFG_SLOT
J30_PROGPARTS	BOOTROM_PROG,SMC_PROG,TPAD_PROG,ENET_PROG,T29ROM:PROG,T29MCU:PROG
J30_DEVEL:ENG	BKLT:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCPLUS_CONN:YES,LOADISNS:YES,DDRVREF_DAC,S0PGOOD_ISL
J30_DEVEL:PVT	LPCPLUS_CONN:YES,XDP_CONN
J30_DEBUG:ENG	DEVEL_BOM,MOJO:YES,XDP,LPCPLUS_R:YES,VREFDQ:M1_M3,VREFCA:LDO_DAC
J30_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,MOJO:YES,XDP,LPCPLUS_R:YES,VREFDQ:M1_M3,VREFCA:LDO,USBHUB2514B
J30_DEBUG:PROD	BKLT:PROD,MOJO:YES,XDP,LPCPLUS_R:YES,LOADISNS:NO,VREFDQ:M1_M3,VREFCA:LDO,USBHUB2513B

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4113	1	IC,IVB,2C,35W,1023BGA	U1000	CRITICAL	CPU_IVB_2C
337S4264	1	IVB,S R0N0,PRQ,L1,2.5,35W,2+2,1.1,3M,BGA	U1000	CRITICAL	CPU_2_5GHZ
337S4265	1	IVB,S R0MU,PRQ,L1,2.9,35W,2+2,1.25,4M,BGA	U1000	CRITICAL	CPU_2_9GHZ
337S4269	1	PANTHERPOINT,C1,SLJ8C,PRQ,BD82HM77	U1800	CRITICAL	
343S0534	1	IC,BCM57765B0,ENET&SD,8X8	U3900	CRITICAL	
338S0753	1	IC,FW643E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
338S1072	1	IC,T29,PRQ,S LJJY,FCBGA,15x15MM,C1	U3600	CRITICAL	T29:YES
353S3055	1	IC,PI3VEDP212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	
946-3827	1	J30 MLB DYMAX ADHESIVE 29993-SC 0.48G	UV_GLUE_J30	CRITICAL	UV_GLUE_J30
516S0806	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,FOXCONN	J3100	CRITICAL	SODIMM:FOXCONN
516-0246	1	CONN,204P,SODIMM,DDR3,P=0.6MM,FOXCONN	J2900	CRITICAL	SODIMM:FOXCONN
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:MOLEX
516-0245	1	CONN,204P,SODIMM,DDR3,P=0.6MM,MOLEX	J2900	CRITICAL	SODIMM:MOLEX
516S0805	1	CONN,204P,SODIMM,SOCKET,DDR3,RAM,BGA,MOLEX	J3100	CRITICAL	SODIMM:HYBRID
516-0246	1	CONN,204P,SODIMM,DDR3,P=0.6MM,FOXCONN	J2900	CRITICAL	SODIMM:HYBRID

Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YG]	CRITICAL	EEEE_F1YG
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YH]	CRITICAL	EEEE_F1YH
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YJ]	CRITICAL	EEEE_F1YJ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YK]	CRITICAL	EEEE_F1YK
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YL]	CRITICAL	EEEE_F1YL
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:F1YM]	CRITICAL	EEEE_F1YM

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0862	1	IC,FLASH,SERIAL,SPI,!MBIT,2V7,REV F	U3990	CRITICAL	ENET_BLANK
341S3096	1	IC ENET,1!MBITFLAH,CIV REV01,K9x	U3990	CRITICAL	ENET_PROG
335S0550	1	IC,EEPROM,SERIAL,SPI,4Kx8,1.8V,MLP8,LF	U3690	CRITICAL	T29ROM:BLANK
341S3430	1	IC,T29 EEPROM,LR,J30/J31	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S3365	1	IC,PROGRMD,T29,PORT MCU,K90IA,K91A,K92A	U9330	CRITICAL	T29MCU:PROG
338S1098	1	IC,SMC12-A3,40MHZ/50DMIPS MCU,9x9,157BGA	U4900	CRITICAL	SMC_BLANK
341S3300	1	IC,SMC,EXTERNAL,FSB,A3,J30	U4900	CRITICAL	SMC_PROG
335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBT,8SOP,FUSE=1	U6100	CRITICAL	BOOTROM_BLANK
335S0812	1	64 MBIT SPI SRL DUAL I/O FLSH,SOIC8	U6100	CRITICAL	BOOTROM_BLANK
341S3558	1	IC,EFI,V00C7,J30/J31	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	
341S3522	1	IC,PSOC,TP/KB,J30/J31	U5701	CRITICAL	TPAD_PROG

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0084		ALL	Delta alt to TDK Magnetics
128S0303	128S0353		ALL	Panasonic alt to Sanyo
138S0676	138S0691		ALL	Murata alt to Samsung
152S0778	152S0693		ALL	Cyntec alt to Vishay
376S0855	376S1032		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S1017		ALL	Rohm alt to Toshiba
376S0937	376S0845		ALL	Fairchild alt to Renesas
376S0777	376S0761		ALL	AON alt to Siliconix
376S0957	376S0958		ALL	Fairchild alt to Fairchild
376S0953	376S0958		ALL	Fairchild alt to Renesas
377S0107	377S0126		ALL	Omsemi alt to Semtech
371S0709	371S0652		ALL	NXP alt to Infineon
514-0788	514-0671		ALL	Acon(w litemi) alt to Acon
607-9310	607-8722		ALL	Renesas alternate to Fairchild
607-9311	607-8723		ALL	Renesas alternate to Fairchild

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1499	152S0864		ALL	Coilcraft alt to Murata
152S1493	152S1300		ALL	Coilcraft alt to Murata
138S0652	138S0648		ALL	Samsung/Murata alt to Taiyo
138S0684	138S0660		ALL	Murata alt to Taiyo
152S1512	152S1295		ALL	Cyntec alt to NEC
152S1019	152S1271		ALL	Cyntec alt to TDKD
376S1023	376S0960		ALL	Siliconix alt to Renesas
353S3312	353S3055		ALL	NXP alt to Pericom
353S3238	353S1428		ALL	Intersil alt to TI
353S3519	353S2179		ALL	Intersil alt to TI
155S0578	155S0367		ALL	Taiyo alt to Murata
138S0681	138S0638		ALL	Taiyo alt to Samsung
138S0671	138S0673		ALL	Taiyo alt to Murata
376S0903	376S0796		ALL	Fairchild alt to Vishay
377S0124	377S0057		ALL	Amotech alt to Tdk
341S3492	341S3096		ALL	Numonix alt to Atmel (ENET ROM)
376S1053	376S0604		ALL	Diodes alt to Fairchild
376S1076	376S0634		ALL	Diodes alt to onsemi

Sub BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-3092	1	J30 MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM
607-8895	1	CMN PTS,PCBA,MLB,J30	CMNPTS	CRITICAL	J30_CMNPTS
607-8721	1	POWER_FETS PAIR,FAIRCHILD,DDR,J30	CSET1	CRITICAL	FET_PAIR
607-8722	1	POWER_FETS PAIR,FAIRCHILD,5V_S3,J30	CSET2	CRITICAL	FET_PAIR
607-8723	1	POWER_FETS PAIR,FAIRCHILD,PBUS_CHARGER,J30	CSET3	CRITICAL	FET_PAIR

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011

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BOM Configuration

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Functional Test Points

Fan Connectors

1812	TRUE	PP5V_S0	6 7
1813	TRUE	FAN_RT_PWM	52
1814	TRUE	FAN_RT_TACH	52

(NEED TO ADD 1 GND TP)

MIC FUNC_TEST

1836	TRUE	BI_MIC_LO	61 62
1835	TRUE	BI_MIC_HI	61 62
1834	TRUE	BI_MIC_SHIELD	61 62

(NEED TO ADD 1 GND TP)

SPEAKER FUNC_TEST

1227	TRUE	SPKRAMP_L_N_OUT	60 61 85
1226	TRUE	SPKRAMP_L_P_OUT	60 61 85
1225	TRUE	SPKRAMP_R_N_OUT	60 61 85
1230	TRUE	SPKRAMP_R_P_OUT	60 61 85
1229	TRUE	SPKRAMP_SUB_N_OUT	60 61 85
1231	TRUE	SPKRAMP_SUB_P_OUT	60 61 85

LVDS FUNC_TEST

1969	TRUE	PP3V3_LCDVDD_SW_F (NEED 2 TP)	6 74
1968	TRUE	PP3V3_S0_LCD_F	6 74
1967	TRUE	PPVOUT_SW_LCDBKLT (NEED 2 TP)	74 77
1489	TRUE	LVDS_DDC_CLK	8 74
1966	TRUE	LVDS_DDC_DATA	8 74
1965	TRUE	LVDS_IG_A_DATA_N<0>	17 74 80
1964	TRUE	LVDS_IG_A_DATA_P<0>	17 74 80
1963	TRUE	LVDS_IG_A_DATA_N<1>	17 74 80
1962	TRUE	LVDS_IG_A_DATA_P<1>	17 74 80
1961	TRUE	LVDS_IG_A_DATA_N<2>	17 74 80
1960	TRUE	LVDS_IG_A_DATA_P<2>	17 74 80
1959	TRUE	LVDS_CONN_A_CLK_F_N	74 85
1958	TRUE	LVDS_CONN_A_CLK_F_P	74 85
1957	TRUE	LED_RETURN_1	74 77
1813	TRUE	LED_RETURN_2	74 77
1956	TRUE	LED_RETURN_3	74 77
1954	TRUE	LED_RETURN_4	74 77
1953	TRUE	LED_RETURN_5	74 77
1952	TRUE	LED_RETURN_6	74 77

(NEED TO ADD 5 GND TP)

SATA ODD CONN

1264	TRUE	PP5V_SW_ODD (NEED 2 TP)	6 41
1266	TRUE	SMC_ODD_DETECT	41 45
1268	TRUE	SATA_ODD_D2R_C_P	41 85
1267	TRUE	SATA_ODD_D2R_C_N	41 85
1265	TRUE	SATA_ODD_R2D_P	41 80
1266	TRUE	SATA_ODD_R2D_N	41 80
1629	TRUE	SMC_SSD_TEMP_CTL_R	
1627	TRUE	HDD_OOB_TEMP	

(NEED TO ADD 3 GND TP)

SATA HDD/IR/SIL

1333	TRUE	PP5V_S0_HDD_FLT (NEED 2 TP)	6 41
1314	TRUE	SATA_HDD_R2D_P	41 80
1313	TRUE	SATA_HDD_R2D_N	41 80
1316	TRUE	SATA_HDD_D2R_C_P	41 80
1317	TRUE	SATA_HDD_D2R_C_N	41 80
1307	TRUE	SYS_LED_ANODE_R	41
1309	TRUE	IR_RX_OUT	41 44
1628	TRUE	SMC_SSD_THROTTLE_R	
1311	TRUE	PP5V_S3_IR_R	41

(NEED TO ADD 3 GND TP)

BATT POWER CONN

1322	TRUE	SMBUS_SMC_5_G3_SCL	6 45 48 84
1321	TRUE	SMBUS_SMC_5_G3_SDA	6 45 48 84
1320	TRUE	SYS_DETECT_L	63
1305	TRUE	PPVBAT_G3H_CONN (NEED 5 TP)	63 64

(NEED TO ADD 5 GND TP)

BIL CONN

1929	TRUE	PP3V42_G3H	6 7
1927	TRUE	SMBUS_SMC_5_G3_SCL	6 45 48 84
1924	TRUE	SMBUS_SMC_5_G3_SDA	6 45 48 84
1926	TRUE	SMC_BIL_BUTTON_L	45 46 63
1908	TRUE	SMC_LID_R	63

(NEED TO ADD 2 GND TP)

X19 CONN

1909	TRUE	PP3V3_WLAN (NEED 3 TP)	6 32 46
1907	TRUE	PCIE_AP_D2R_PI_P	32 81
1906	TRUE	PCIE_AP_D2R_PI_N	32 81
1905	TRUE	PCIE_AP_R2D_P	32 81
1904	TRUE	PCIE_AP_R2D_N	32 81
1903	TRUE	PCIE_CLK100M_AP_CONN_P	32 85
1902	TRUE	PCIE_CLK100M_AP_CONN_N	32 85
1900	TRUE	PP3V3_S3RS4_BT_F	32
1899	TRUE	PCIE_WAKE_L	17 24 32
1922	TRUE	USB_BT_CONN_P	32 80
1920	TRUE	USB_BT_CONN_N	32 80
1972	TRUE	AP_CLKREQ_Q_L	32
1918	TRUE	AP_RESET_CONN_L	32
1629	TRUE	AP_TEMP_SMB_SDA_R	32
1628	TRUE	AP_TEMP_SMB_SCL_R	32
1630	TRUE	WIFI_EVENT_L_R	32

(NEED TO ADD 5 GND TP)

IPD_FLEX_CONN

1975	TRUE	PP3V3_S4	6 7
1974	TRUE	PP18V5_Z2	6 54
1973	TRUE	Z2_CS_L	53 54
1972	TRUE	Z2_DEBUG3	53 54
1971	TRUE	Z2_MOSI	53 54
1970	TRUE	Z2_MISO	53 54
1969	TRUE	Z2_SCLK	53 54
1968	TRUE	Z2_BOOST_EN	54
1967	TRUE	Z2_HOST_INTN	53 54
1966	TRUE	Z2_CLKIN	53 54
1965	TRUE	Z2_KEY_ACT_L	53 54
1964	TRUE	Z2_RESET	53 54
1962	TRUE	PSOC_MISO	53 54
1960	TRUE	PSOC_MOSI	53 54
1959	TRUE	PSOC_SCLK	53 54
1957	TRUE	SMBUS_SMC_2_S3_SCL	6 45 48 84
1956	TRUE	SMBUS_SMC_2_S3_SDA	6 45 48 84
1977	TRUE	PSOC_F_CS_L	53 54
1540	TRUE	PICKB_L	53 54
1626	TRUE	PP5V_S5_CUMULUS	54

(NEED TO ADD 2 GND TP)

KEYBOARD CONN

1934	TRUE	PP3V3_S4	6 7
1935	TRUE	PP3V42_G3H	6 7
1944	TRUE	WS_KBD1	53
1945	TRUE	WS_KBD2	53
1946	TRUE	WS_KBD3	53
1947	TRUE	WS_KBD4	53
1948	TRUE	WS_KBD5	53
1949	TRUE	WS_KBD6	53
1950	TRUE	WS_KBD7	53
1951	TRUE	WS_KBD8	53
1952	TRUE	WS_KBD9	53
1953	TRUE	WS_KBD10	53
1323	TRUE	WS_KBD11	53
1329	TRUE	WS_KBD12	53
1328	TRUE	WS_KBD13	53
1327	TRUE	WS_KBD14	53
1343	TRUE	WS_KBD15_CAP	53
1342	TRUE	WS_KBD16_NUM	53
1341	TRUE	WS_KBD17	53
1335	TRUE	WS_KBD18	53
1340	TRUE	WS_KBD19	53
1339	TRUE	WS_KBD20	53
1338	TRUE	WS_KBD21	53
1337	TRUE	WS_KBD22	53
1336	TRUE	WS_KBD23	53
1334	TRUE	WS_KBD_ONOFF_L	53
1332	TRUE	WS_LEFT_SHIFT_KBD	53
1330	TRUE	WS_LEFT_OPTION_KBD	53
1331	TRUE	WS_CONTROL_KBD	53

(NEED TO ADD 2 GND TP)

KBD BACKLIGHT CONN

1356	TRUE	KBDLED_ANODE	54
1354	TRUE	SMC_KDBLED_PRESENT_L	54

(NEED TO ADD 1 GND TP)

CAMERA/ALS CONN

1408	TRUE	PP5V_S3_ALSCAMERA_F	32
1409	TRUE	SMBUS_SMC_2_S3_SCL	6 45 48 84
1410	TRUE	SMBUS_SMC_2_S3_SDA	6 45 48 84
1707	TRUE	USB_CAMERA_CONN_P	32 80
1706	TRUE	USB_CAMERA_CONN_N	32 80

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

1797	TRUE	PPVCORE_S0_CPU	7
1795	TRUE	PPVCORE_S0_AXG	7
1434	TRUE	PP1V2_S3_ENET_INTREG	71
1789	TRUE	PP1V05_S0	7
1793	TRUE	PP1V5_S3RS0	7 85
1792	TRUE	PP1V8_S0	7
1791	TRUE	PP3V3_S0	7 85
1790	TRUE	PP5V_S0	6 7
1575	TRUE	PP3V3_S3	7
1573	TRUE	PP5V_S3	7
1572	TRUE	PPVCCSA_S0_CPU	7
1410	TRUE	PP3V3_S5	7 85
1577	TRUE	PP3V42_G3H	6 7
1574	TRUE	PPBUS_G3H	7
1576	TRUE	PP3V3_ENET	7
1417	TRUE	PP3V3_WLAN	6 32 46
1922	TRUE	PP5V_SW_ODD	6 41
1921	TRUE	PP5V_S0_HDD_FLT	6 41
1199	TRUE	PP18V5_Z2	6 54
1198	TRUE	PP3V3_S0_LCD_F	6 74
1410	TRUE	PP3V3_LCDVDD_SW_F	6 74
1189	TRUE	PP4V5_AUDIO_ANALOG	57 62
1188	TRUE	PP1V5_S3	7
1410	TRUE	SMC_PM_G2_EN	45 73
1187	TRUE	PM_SLP_S4_L	17 26 32 45 73
1506	TRUE	PM_SLP_S3_L	8 17 26 45 73
1186	TRUE		

(NEED TO ADD 6 GND TP)

DC POWER CONN

(NEED 3 TP)

1912	TRUE	PP18V5_DCIN_FUSE	63
1904	TRUE	ADAPTER_SENSE	63

(NEED TO ADD 4 GND TP)

LPC+SPI DEBUG_CONN

1658	TRUE	LPC_AD<0>	16 45 47 81
1657	TRUE	LPC_AD<1>	16 45 47 81
1656	TRUE	LPC_AD<2>	16 45 47 81
1640	TRUE	LPC_AD<3>	16 45 47 81
1660	TRUE	LPC_CLK33M_LPCPLUS	24 47 81
1661	TRUE	LPC_FRAME_L	16 45 47 81
1662	TRUE	LPC_PWRDWN_L	17 45 47
1663	TRUE	LPC_SERIRQ	16 45 47
1664	TRUE	LPCPLUS_GPIO	19 47
1665	TRUE	LPCPLUS_RESET_L	24 47
1666	TRUE	PM_CLKRUN_L	17 45 47
1667	TRUE	PP3V42_G3H	6 7
1668	TRUE	PP5V_S0	6 7
1610	TRUE	SMC_RX_L	45 46 47
1611	TRUE	SMC_TCK	45 46 47
1612	TRUE	SMC_TDI	45 46 47
1613	TRUE	SMC_TDO	45 46 47
1615	TRUE	SMC_TMS	45 46 47
1637	TRUE	SMC_TX_L	45 46 47
1616	TRUE	SPI_ALT_CLK	47
1618	TRUE	SPI_ALT_CS_L	47
1620	TRUE	SPI_ALT_MISO	47
1619	TRUE	SPI_ALT_MOSI	47
1692	TRUE	SPIROM_USE_MLB	19 47 56

(NEED TO ADD 2 GND TP)

NC NO_TESTs

NO_TEST

17	TP_CRT_IG_BLUE	MAKE_BASE=TRUE	NC_CRT_IG_BLUE
17	TP_CRT_IG_GREEN	MAKE_BASE=TRUE	NC_CRT_IG_GREEN
17	TP_CRT_IG_RED	MAKE_BASE=TRUE	NC_CRT_IG_RED
17	TP_CRT_IG_DDC_CLK	MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK
17	TP_CRT_IG_DDC_DATA	MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA
17	TP_CRT_IG_HSYNC	MAKE_BASE=TRUE	NC_CRT_IG_HSYNC
17	TP_CRT_IG_VSYNC	MAKE_BASE=TRUE	NC_CRT_IG_VSYNC
17	TP_LVDS_IG_CTRL_CLK	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK
17	TP_LVDS_IG_CTRL_DATA	MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA
17	TP_PCH_LVDS_VBG	MAKE_BASE=TRUE	NC_PCH_LVDS_VBG
16	TP_HDA_SDIN1	MAKE_BASE=TRUE	NC_HDA_SDIN1
16	TP_HDA_SDIN2	MAKE_BASE=TRUE	NC_HDA_SDIN2
16	TP_HDA_SDIN3	MAKE_BASE=TRUE	NC_HDA_SDIN3
18	TP_PCI_PME_L	MAKE_BASE=TRUE	NC_PCI_PME_L
18	TP_PCI_CLK33M_OUT3	MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3
16	TP_CLINK_CLK	MAKE_BASE=TRUE	NC_CLINK_CLK
16	TP_CLINK_DATA	MAKE_BASE=TRUE	NC_CLINK_DATA
16	TP_CLINK_RESET_L	MAKE_BASE=TRUE	NC_CLINK_RESET_L
16	TP_PCIE_CLK100M_PEBN	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN
16	TP_PCIE_CLK100M_PEBP	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP
38	TP_FW643_SDA	MAKE_BASE=TRUE	NC_FW643_SDA
38	TP_FW643_SM	MAKE_BASE=TRUE	NC_FW643_SM
38	TP_FW643_TCK	MAKE_BASE=TRUE	NC_FW643_TCK
38	TP_FW643_TMS	MAKE_BASE=TRUE	NC_FW643_TMS
38	TP_FW643_FW620_L	MAKE_BASE=TRUE	NC_FW643_FW620_L
38	TP_FW643_VBUF	MAKE_BASE=TRUE	NC_FW643_VBUF
38	TP_FW643_OCR10_CTL	MAKE_BASE=TRUE	NC_FW643_OCR10_CTL
38	TP_FW643_AVREG	MAKE_BASE=TRUE	NC_FW643_AVREG
38	TP_FW643_TDI	MAKE_BASE=TRUE	NC_FW643_TDI
23	TP_XDP_PCH_OBSFN_A<0..1>	MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>
23	TP_XDP_PCH_OBSFN_B<0..1>	MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>
23	TP_XDPPCH_HOOK2	MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK2
23	TP_XDPPCH_HOOK3	MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK3
23	TP_XDP_PCH_OBSFN_D<0..1>	MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>
23	TP_XDP_PCH_HOOK4	MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4
23	TP_XDP_PCH_HOOK5	MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK5
16	TP_PCH_GPIO64_CLKOUTFLEX0	MAKE_BASE=TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
16	TP_PCH_GPIO65_CLKOUTFLEX1	MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
16	TP_PCH_GPIO66_CLKOUTFLEX2	MAKE_BASE=TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
16	TP_PCH_GPIO67_CLKOUTFLEX3	MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3

NC NO_TESTs

NO_TEST

1660	TRUE	NC_FW2_TPBP	40
1659	TRUE	NC_FW2_TPBN	40
1658	TRUE	NC_FW2_TPBIAS	40
1657	TRUE	NC_FW2_TPAP	40
1656	TRUE	NC_FW2_TPAN	40
1655	TRUE	NC_FW0_TPBP	40
1654	TRUE	NC_FW0_TPBN	40
1653	TRUE	NC_FW0_TPAP	40
1602	TRUE	XDP_PCH_AP_PWR_EN	
1603	TRUE	XDP_PCH_USB_HUB_SOFT_RST_L	
1604	TRUE	XDP_PCH_SDCONN_STATE_RST_L	
1680	TRUE	XDP_PCH_ENET_PWR_EN	
1652	TRUE	XDP_PCH_SDCONN_DET_L	
1683	TRUE	XDP_PCH_S5_PWRGD	23
1684	TRUE	XDP_PCH_PWRBTN_L	23
1685	TRUE	XDP_PCH_ISOLATE_CPU_MEM_L	
1686	TRUE	XDP_FW_CLKREQ_L	
1688	TRUE	XDP_AP_CLKREQ_L	
1687	TRUE	XDP_PCH_AUD_IPHS_SWITCH_EN	

17	TP_SDVO_TVCLKINN	MAKE_BASE=TRUE	NC_SDVO_TVCLKINN
17	TP_SDVO_TVCLKINP	MAKE_BASE=TRUE	NC_SDVO_TVCLKINP
17	TP_SDVO_STALLN	MAKE_BASE=TRUE	NC_SDVO_STALLN
17	TP_SDVO_STALLP	MAKE_BASE=TRUE	NC_SDVO_STALLP
17	TP_SDVO_INTN	MAKE_BASE=TRUE	NC_SDVO_INTN
17	TP_SDVO_INTP	MAKE_BASE=TRUE	NC_SDVO_INTP

	NC_EDP_TXP<0..3>	MAKE_BASE=TRUE	TP_EDP_TX_P<0..3> 9
	NC_EDP_TXN<0..3>	MAKE_BASE=TRUE	TP_EDP_TX_N<0..3> 9
	NC_EDP_AUXP	MAKE_BASE=TRUE	TP_EDP_AUX_P 9
	NC_EDP_AUXN	MAKE_BASE=TRUE	TP_EDP_AUX_N 9
	NC_CPU_THERMDA	MAKE_BASE=TRUE	TP_CPU_THERMDA
	NC_CPU_THERMDC	MAKE_BASE=TRUE	TP_CPU_THERMDC
	NC_CPU_RSVD<30..45>	MAKE_BASE=TRUE	TP_CPU_RSVD<30..45>
	NC_CPU_RSVD<8..27>	MAKE_BASE=TRUE	TP_CPU_RSVD<8..27>
	NC_PEG_R2D_CP<0..7>	MAKE_BASE=TRUE	=PEG_R2D_C_P<0..7> 9
	NC_PEG_R2D_CN<0..7>	MAKE_BASE=TRUE	=PEG_R2D_C_N<0..7> 9
	NC_PEG_D2RP<0..7>	MAKE_BASE=TRUE	=PEG_D2R_P<0..7> 9
	NC_PEG_D2RN<0..7>	MAKE_BASE=TRUE	=PEG_D2R_N<0..7> 9
	NC_PEG_R2D_CP<8..11>	MAKE_BASE=TRUE	=PEG_R2D_C_P<8..11> 9
	NC_PEG_R2D_CN<8..11>	MAKE_BASE=TRUE	=PEG_R2D_C_N<8..11> 9
	NC_PEG_D2RP<8..11>	MAKE_BASE=TRUE	=PEG_D2R_P<8..11> 9
	NC_PEG_D2RN<8..11>	MAKE_BASE=TRUE	=PEG_D2R_N<8..11> 9
16	TP_PCIE_CLK100M_PE4N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N
16	TP_PCIE_CLK100M_PE4P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P
16	TP_PCIE_CLK100M_PE5N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N
16	TP_PCIE_CLK100M_PE5P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P
	TP_PCIE_CLK100M_PE6N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N
	TP_PCIE_CLK100M_PE6P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P
	TP_PCIE_CLK100M_PE7N	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N
	TP_PCIE_CLK100M_PE7P	MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P
53	TP_PSOC_P1_3	MAKE_BASE=TRUE	NC_PSOC_P1_3
16	TP_SATA_C_D2RN	MAKE_BASE=TRUE	NC_SATA_C_D2RN
16	TP_SATA_C_D2RP	MAKE_BASE=TRUE	NC_SATA_C_D2RP
16	TP_SATA_C_R2D_CN	MAKE_BASE=TRUE	NC_SATA_C_R2D_CN
16	TP_SATA_C_R2D_CP	MAKE_BASE=TRUE	NC_SATA_C_R2D_CP
16	TP_SATA_D_D2RN	MAKE_BASE=TRUE	NC_SATA_D_D2RN
16	TP_SATA_D_D2RP	MAKE_BASE=TRUE	NC_SATA_D_D2RP
16	TP_SATA_D_R2D_CN	MAKE_BASE=TRUE	NC_SATA_D_R2D_CN
16	TP_SATA_D_R2D_CP	MAKE_BASE=TRUE	NC_SATA_D_R2D_CP
16	TP_SATA_E_D2RN	MAKE_BASE=TRUE	NC_SATA_E_D2RN
16	TP_SATA_E_D2RP	MAKE_BASE=TRUE	NC_SATA_E_D2RP
16	TP_SATA_E_R2D_CN	MAKE_BASE=TRUE	NC_SATA_E_R2D_CN
16	TP_SATA_E_R2D_CP	MAKE_BASE=TRUE	NC_SATA_E_R2D_CP
16	TP_SATA_F_D2RN	MAKE_BASE=TRUE	NC_SATA_F_D2RN
16	TP_SATA_F_D2RP	MAKE_BASE=TRUE	NC_SATA_F_D2RP
16	TP_SATA_F_R2D_CN	MAKE_BASE=TRUE	NC_SATA_F_R2D_CN
16	TP_SATA_F_R2D_CP	MAKE_BASE=TRUE	NC_SATA_F_R2D_CP
33	TP_TBT_MONDC0	MAKE_BASE=TRUE	NC_TBT_MONDC0
33	TP_TBT_MONDC1	MAKE_BASE=TRUE	NC_TBT_MONDC1
33	TP_TBT_MONOBSP	MAKE_BASE=TRUE	NC_TBT_MONOBSP
33	TP_TBT_MONOBSN	MAKE_BASE=TRUE	NC_TBT_MONOBSN
33	TP_DP_T29SRC_ML_CP<0..3>	MAKE_BASE=TRUE	NC_DP_T29SRC_ML_CP<0..3>
33	TP_DP_T29SRC_ML_CN<0..3>	MAKE_BASE=TRUE	NC_DP_T29SRC_ML_CN<0..3>
33	TP_DP_T29SRC_AUXCH_CP	MAKE_BASE=TRUE	NC_DP_T29SRC_AUXCH_CP
33	TP_DP_T29SRC_AUXCH_CN	MAKE_BASE=TRUE	NC_DP_T29SRC_AUXCH_CN
33 6	TP_T29_PCIE_RESET0_L	MAKE_BASE=TRUE	TP_T29_PCIE_RESET0_L 6 33
33 6	TP_T29_PCIE_RESET1_L	MAKE_BASE=TRUE	TP_T29_PCIE_RESET1_L 6 33
33 6	TP_T29_PCIE_RESET2_L	MAKE_BASE=TRUE	TP_T29_PCIE_RESET2_L 6 33
33 6	TP_T29_PCIE_RESET3_L	MAKE_BASE=TRUE	TP_T29_PCIE_RESET3_L 6 33
1692	PCH_VSS_NCTF<1>		81
1523	PCH_VSS_NCTF<2>		81
1520	PCH_VSS_NCTF<5>		81
1519	PCH_VSS_NCTF<9>		81
1518	PCH_VSS_NCTF<11>		81
1517	PCH_VSS_NCTF<12>		81
1647	PCH_VSS_NCTF<15>		81
1646	PCH_VSS_NCTF<17>		81
1645	PCH_VSS_NCTF<19>		6 81
1644	PCH_VSS_NCTF<19>		6 81
1643	PCH_VSS_NCTF<21>		81
1642	PCH_VSS_NCTF<25>		81
1641	PCH_VSS_NCTF<27>		81
1640	PCH_VSS_NCTF<29>		81
8	TP_LVDS_IG_B_CLKN	TRUE	NC_LVDS_IG_B_CLKN
8	TP_LVDS_IG_B_CLKP	MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP
	TP_LVDS_IG_BKL_PWM	MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM
	SMC_BS_ALRT_L	MAKE_BASE=TRUE	NC_SMC_BS_ALRT_L

SYNC_MASTER=K90I_MLB

PAGE TITLE

FUNC TEST

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DRAWING NUMBER 051-9058 SIZE D

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BRANCH

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"G3Hot" (Always-Present) Rails

64 63 =PPBUS_G3H — PPBUS_G3H
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPBUS_S0_LCDBKLT 77
- =PPBUS_S5_FWPWRSW 39
- =PPBUS_S0_VSENSE 50
- =PPVIN_SW_T29BST 8 35
- =PPVIN_S5_HS_COMPUTING_ISNS_R 50
- =PPVIN_S5_HS_OTHER_ISNS_R 50

35 PPVIN_SW_T29BST
VOLTAGE=12.6V

50 =PPVIN_S5_HS_COMPUTING_ISNS — PPBUS_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPVIN_S0_CPUIMVP 68 69
- =PPVIN_S3_DDRREG 67
- =PPVIN_S0_CPUVCCIOS0 70
- =PPVIN_S0_VCCSAS0 65
- =PPVIN_S0_CPUAXG 69

50 =PPVIN_S5_HS_OTHER_ISNS — PPBUS_S5_HS_OTHER_ISNS
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPVIN_S5_5VS3 66
- =PPVIN_S5_3V3S5 66

63 =PP18V5_DCIN_CONN — PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=18.5V
MAKE_BASE=TRUE
- =PPDCIN_S5_CHGR 64
- =PPDCIN_S5_VSENSE 50

63 =PP3V42_G3H_REG — PP3V42_G3H 6
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.42V
MAKE_BASE=TRUE
- =PP3V3_S5_LPCPLUS 47
- =PP3V3_S5_SMC 45 46
- =PP3V42_G3H_BATT 63
- =PP3V42_G3H_CHGR 64
- =PP3V42_G3H_ONEWIREPROT 63
- =PP3V42_G3H_PWRCTL 73
- =PP3V42_G3H_SMBUS_SMC_BSA 48
- =PP3V42_G3H_SMCUSBMUX 42
- =PP3V42_G3H_TPAD 53
- =PPVIN_S5_SMCVREF 46
- =PPVBAT_G3_SYSCLK 24
- =PP3V42_G3H_AUDIO 58

24 =PPVRTC_G3_OUT — PPVRTC_G3H
MIN_LINE_WIDTH=0.2 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3V
MAKE_BASE=TRUE
- =PPVRTC_G3_PCH 16 17 20

5V Rails

66 =PP5V_S5_LDO — PP5V_S5
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S5_P1V5DDRFET 72
- =PP5V_S5_TPAD 54
- =PP5V_S5_P5VSUSFET 72

72 =PP5V_SUS_FET — PP5V_SUS
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP5V_SUS_PCH 22

66 =PP5V_S3_REG — PP5V_S3 6
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S3_ALSCAMERA 32
- =PP5V_S3_AUDIO 57
- =PP5V_S3_AUDIO_AMP 60
- =PP5V_S3_DDRREG 67
- =PP5V_S3_IR 41 44
- =PP5V_S3_MEMRESET 26
- =PP5V_S3_ODD 41
- =PP5V_S3_P5VS0FET 72
- =PP5V_S3_USB 42
- =PP5V_S3_SYSLED 46

72 =PP5V_S0_FET — PP5V_S0 6
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_BKL 77
- =PP5V_S0_CPUIMVP 68 69
- =PP5V_S0_CPUVCCIOS0 70
- =PP5V_S0_FAN_RT 52
- =PP5V_S0_HDD_ISNS_R 49
- =PP5V_S0_KBDLED 54
- =PP5V_S0_LPCPLUS 47
- =PP5V_S0_VCCSAS0 65
- =PP5V_S0_PCH 22 24
- =PP5V_S0_VMON 73
- =PP5V_S0_ISNS 49
- =PP5V_S0_AUDIO

49 =PP5V_S0_HDD_ISNS — PP5V_S0_HDD
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.4MM
VOLTAGE=5V
MAKE_BASE=TRUE
- =PP5V_S0_HDD 41

3.3V Rails

66 =PP3V3_S5_REG — PP3V3_S5
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
- =PP3V3_S5_XDP 23
- =PP3V3_S0_P3V3S0FET 72
- =PP3V3_S3_P3V3S3FET 72
- =PP3V3_S5_CPU_VCCDDR 26
- =PP3V3_S4_P3V3S4FET 72
- =PP3V3_S5_LCD 74
- =PP3V3_S5_PCH 17
- =PP3V3_S5_PCHPWRGD 24
- =PP3V3_S5_SMCBATLOW 46
- =PP3V3_S5_PCH_VCCDSW 20 22
- =PP3V3_S5_SYSCLK 24
- =PP3V3_S5_VMON 73
- =PP3V3_S5_PWRCTL 73
- =PP3V3_S5_P3V3SUSFET 72
- =PP3V3_S4_TBTAPWRSW 76
- =PP3V3_S5_PCH_GPIO 19

72 =PP3V3_SUS_FET — PP3V3_SUS
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_SUS_PCH_VCCSUS_USB 20 22
- =PP3V3_SUS_PCH_VCCSUS_GPIO 20 22
- =PP3V3_SUS_PCH_VCCSUS 20
- =PP3V3_SUS_PCH_GPIO 16 17 18 19
- =PP3V3_SUS_PCH 22
- =PP3V3_SUS_PWRCTL 73
- =PP3V3_SUS_P1V05SUSLDO 71
- =PP3V3_SUS_SMC 46
- =PP3V3_SUS_ROM 56
- =PP3V3_SUS_PCH_VCC_SPI 20 22

72 =PP3V3_S4_FET — PP3V3_S4 6
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S4_TPAD 53 54
- =PP3V3_S4_SMC 46
- =PP3V3_S4_SD_HPD 30
- =PP3V3_S4_BT 32

72 =PP3V3_S3_FET — PP3V3_S3 6
MIN_LINE_WIDTH=0.50MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S3_BT 32
- =PP3V3_S3_MEMRESET 26
- =PP3V3_S3_SMBUS_SMC_A_S3 48
- =PP3V3_S3_SMBUS_SMC_MGMT 48
- =PP3V3_S3_SMS 55
- =PP3V3_S3_USB_HUB 25
- =PP3V3_S3_USB_RESET 25
- =PP3V3_S3_VREFMRGN 31
- =PP3V3_S3_WLAN 32
- =PP3V3_S3_SDBUF 24
- =PP3V3_S3_P3V3ENETFET 73
- =PP3V3_S3_PCH_GPIO 18 24
- =PP3V3_S3_ISNS 49
- =PP3V3_S3_USBMUX 25

72 =PP3V3_S0_FET — PP3V3_S0 6 85
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.20MM MAKE_BASE=TRUE
- =PP3V3_S0_HDD 41
- =PP3V3_S0_AUDIO 57 61 62
- =PP3V3_S0_BKL_VDDIO 77
- =PP3V3_S0_ISNS 49
- =PP3V3_S0_HS_COMPUTING_ISNS 50
- =PP3V3_S0_CPUTHMSNS 51
- =PP3V3_S0_LCD 74
- =PP3V3_S0_DP_DDC 8
- =PP3V3_S0_ENETPHY 36
- =PP3V3_S0_FAN_RT 52
- =PP3V3_S0_FWPWRCTL 39
- =PP3V3_S0_FWLATEVG 39 40
- =PP3V3_S0_P3V3T29FET 35
- =PP3V3_S0_SDCARD 30
- =PP3V3_S0_P1V8S0 71
- =PP3V3_S0_ODD 41
- =PP3V3_FW_P3V3FWFET 39
- =PP3V3_S0_PCH 16 22
- =PP3V3_S0_PCH_GPIO 16 17 18 19 30
- =PP3V3_S0_PCH_VCC3_3_CLK 22
- =PP3V3_S0_PCH_VCC3_3_GPIO 20 22
- =PP3V3_S0_PCH_VCC3_3_HVCMOS 20 22
- =PP3V3_S0_PCH_VCC3_3_PCI 20 22
- =PP3V3_S0_PCH_VCC3_3_SATA 20 22
- =PP3V3_S0_PCH_VCCADAC 22
- =PP3V3_S0_PCH_VCCA_LVDS 20
- =PP3V3_S0_PWRCTL 73
- =PP3V3_S0_RSTBUF 24
- =PP3V3_S0_SB_PM 24
- =PP3V3_S0_SMBUS_PCH 48
- =PP3V3_S0_SMBUS_SMC_0_S0 48
- =PP3V3_S0_SMBUS_SMC_B_S0 48
- =PP3V3_S0_SMC 41
- =PP3V3_S0_KBDLED 54
- =PP3V3_S0_VMON 73
- =PPSPD_S0_MEM_A 27
- =PPSPD_S0_MEM_B 29
- =PP3V3_S0_P1V5S0 71
- =PP3V3_S0_T29PWRCTL 35
- =PP3V3_S0_HS_OTHER_ISNS 50
- =PP3V3_S0_DPSDRVA 75
- =PP3V3_S0_P1V05S0LDO 71
- =PP3V3_S0_IMVPISNS 49
- =PP3V3_S0_XDP 23
- =PP3V3_S0_T29I2C 48

1.8V/1.5V/1.2V/1.05V Rails

71 =PP1V8_S0_REG — PP1V8_S0 6
2A max supply
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE
- =PP1V8_S0_CPU_VCCPLL 14
- =PP1V8_S0_PCH_VCCTX_LVDS 22
- =PP1V8_S0_PCH_VCC_DFTERM 19 20 22
- =PP1V8_S0_P1V05S0LDO 71
- =PP1V8R1V5_S0_PCH_VCCVRM 20
- =PPVDDIO_S0_SBCLK 24

49 =PP1V5_S3_DDR_ISNS — PP1V5_S3_DDR
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_MEMRESET 26
- =PP1V5_S3_MEM_A 27
- =PP1V5_S3_MEM_B 29
- =PPVIN_S0_DDRREG_LDO 67
- =PPDDR_S3_MEMVREF 31

67 =PPDDR_S3_REG — PP1V5_S3 6
MIN_LINE_WIDTH=0.8 MM
MIN_NECK_WIDTH=0.1 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_P1V5S3RS0_FET 72
- =PP1V5_S3_DDR_ISNS_R 49

72 =PP1V5_S3RS0_FET — PP1V5_S3RS0 6 85
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S3_CPU_VCCDDR 10 12 15 26

71 =PP1V5_S0_REG — PP1V5_S0
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
- =PP1V5_S0_RDRVR 41
- =PP1V8R1V5_S0_AUDIO 57
- =PP3V3R1V5_S0_AUDIO 57
- =PP3V3R1V5_S0_PCH_VCCSUSHDA 20 22 24
- =PP1V5_S0_VMON 73

67 31 =PPVTT_S3_DDR_BUF — PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.75V
MAKE_BASE=TRUE

67 =PPVTT_S0_DDR_LDO — PP0V75_S0_DDRVTT
MIN_LINE_WIDTH=2 mm
MIN_NECK_WIDTH=0.17 mm
VOLTAGE=0.75V
MAKE_BASE=TRUE
- =PP0V75_S0_MEM_VTT_A 27
- =PP0V75_S0_MEM_VTT_B 29
- =PPVTT_S0_VTTCLAMP 26

65 =PPVCCSA_S0_REG — PPVCCSA_S0_CPU 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=0.9V
MAKE_BASE=TRUE
- =PPVCCSA_S0_CPU 12 15

71 =PP1V05_SUS_LDO — PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_SUS_PCH_JTAG 23

70 =PPCPUVCCIO_S0_REG — PP1V05_S0 6
? mA
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1V
MAKE_BASE=TRUE
- =PP1V05_S0_CPU_VCCIO 9 10 12 14
- =PPVCCIO_S0_CPUIMVP 68
- =PPVCCIO_S0_XDP 23
- =PPVCCIO_S0_SMC 46
- =PP1V05_S0_FWPWRCTL 39
- =PP1V05_FW_P1V0FWFET 39
- =PP1V05_S0_VMON 73
- =PP1V05_S0_P1V05T29FET 35

XW0800 SM 1 2
XW0801 SM 1 2

PP1V05_S0_PCH
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1V
MAKE_BASE=TRUE
- =PP1V05_S0_PCH_VCCIO_PLLPCIE 20
- =PP1V05_S0_PCH 16 22
- =PP1V05_S0_PCH_VCCIO 20 22
- =PP1V05_S0_PCH_VCCIO_PCIE 17
- =PP1V05_S0_PCH_VCCIO_SATA 16 20 22
- =PP1V05_S0_PCH_VCCASW 20 22
- =PP1V05_S0_PCH_VCCIO_USB 20 22
- =PP1V05_S0_PCH_VCC_CORE 20 22
- =PP1V05_S0_PCH_VCCIO_CLK 20 22
- =PP1V05_S0_PCH_VCCDIFFCLK 16 20 22
- =PP1V05_S0_PCH_VCCSSC 20 22
- =PP1V05_S0_PCH_V_PROC_IO 20 22
- =PP1V05_S0_PCH_VCCIO_PLLUSB 20
- =PP1V05_S0_PCH_VCC_DMI 20 22
- =PP1V05_S0_PCH_VCCIO_PLLFDI 20
- =PP1V05_S0_PCH_VCCDMI_FDI 20

ENET Rails

73 =PP3V3_ENET_FET — PP3V3_ENET 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_ENET_PHY 24 36 71
- =PP3V3_ENET_SYSCLK 24
- =PPVDDIO_ENET_CLK 24

"FW" (FireWire) Rails

39 =PPBUS_FW_FET — PPVP_FW
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=12.6V
MAKE_BASE=TRUE
- =PPVP_FW_PORT1 40
- =PPVP_FW_PHY_CPS_FET 40

39 =PP3V3_FW_FET — PP3V3_FW_FWPHY
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PP3V3_FW_FWPHY 38 39 40
- =PP3V3_S0_P1V05FWFET

39 =PP1V0_FW_FET_R — PP1V0_FW_FWPHY
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
MAKE_BASE=TRUE
- =PP1V0_FW_FWPHY 38 39

T29 Rails (off when no cable)

35 8 =PP15V_T29_REG — PP15V_T29
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=17.8V
MAKE_BASE=TRUE
- =PPHV_SW_TBTAPWRSW 76

35 =PP3V3_T29_FET — PP3V3_T29
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
- =PPVDDIO_T29_CLK 24
- =PP3V3_T29_RTR 33 34 35
- =PP3V3_T29_PCH_GPIO 16 19

35 =PP1V05_T29_FET — PP1V05_T29
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_T29_RTR 34

1V05 S0 LDO

71 =PP1V05_S0_LDO — PP1V05_S0_PCH_VCCADPLL
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PP1V05_S0_PCH_VCCADPLL 22

Chipset "VCore" Rails

69 =PPVCORE_S0_CPU_REG — PPVCORE_S0_CPU 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.25V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU 9 12 14
- =PPCPUVCORE_S0_VSENSE 49

69 =PPVCORE_S0_AXG_REG — PPVCORE_S0_AXG 6
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE
- =PPVCORE_S0_CPU_VCCAXG 9 12 15
- =PPAXGVCORE_S0_VSENSE 49

15 12 =PP1V5_S3_CPU_VCCDQ — PP1V5_S3_CPU_VCCDQ
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE

14 12 8 =PP1V05_S0_CPU_VCCPQE — PP1V05_S0_CPU_VCCPQE
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

14 12 =PP1V8_S0_CPU_VCCPLL_R — PP1V8_S0_CPU_VCCPLL_R
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
MAKE_BASE=TRUE

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Power Aliases

Apple Inc.

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HEATSINK STANDOFFS

Z0902 STDOFF-4.50D.98H-1.1-3.48-TH

Z0904 STDOFF-4.50D.98H-1.1-3.48-TH — BELOW CPU

Z0920 STDOFF-4.50D.98H-1.1-3.48-TH — LEFT OF CPU

FAN STANDOFF

Z0905 STDOFF-4.50D.98H-1.1

MLB MOUNTING (TO C. BRACKET) SCREW HOLE

OMIT Z0906 3R2P5

MLB MOUNTING (TO TOPCASE) SCREW HOLES

OMIT Z0908 3R2P5
OMIT Z0909 3R2P5
OMIT Z0910 3R2P5
OMIT Z0911 3R2P5
OMIT Z0912 3R2P5

EMI IO (SHORT) POGO PINS

ZS0900 1.4DIA-SHORT-SILVER-K99
ZS0901 1.4DIA-SHORT-SILVER-K99
ZS0910 1.4DIA-SHORT-SILVER-K99
ZS0903 1.4DIA-SHORT-SILVER-K99

EMI TALL POGO PINS

ZS0904 POGO-2.00D-3.5H-K86-K87
ZS0905 POGO-2.00D-3.5H-K86-K87
ZS0907 POGO-2.00D-3.5H-K86-K87

TALL POGO PINS close to DIMM conn.

ZS0920 POGO-2.00D-3.5H-K86-K87 — NO STUFF
ZS0921 POGO-2.00D-3.5H-K86-K87 — NO STUFF
ZS0922 POGO-2.00D-3.5H-K86-K87 — NO STUFF
ZS0923 POGO-2.00D-3.5H-K86-K87 — NO STUFF
ZS0924 POGO-2.00D-3.5H-K86-K87 — NO STUFF

CPU signals

MEMVTT_EN		=DDRVTT_EN
DP_EXTA_ML_C_P<3..0>		TP_DP_IG_B_MLP<3..0>
DP_EXTA_ML_C_N<3..0>		TP_DP_IG_B_MLN<3..0>
DP_EXTA_AUXCH_C_P		DPA_IG_AUX_CH_P
DP_EXTA_AUXCH_C_N		DPA_IG_AUX_CH_N
FW_PLUG_DET_L		FW_PME_L
FW643_WAKE_L		=FW_PME_L
TP_SMC_EXCARD_PWR_EN		SMC_EXCARD_PWR_EN
PCIE_EXCARD_D2R_N		NC_PCIE_EXCARD_D2RN
PCIE_EXCARD_D2R_P		NC_PCIE_EXCARD_D2RP
PCIE_EXCARD_R2D_C_N		NC_PCIE_EXCARD_R2D_CN
PCIE_EXCARD_R2D_C_P		NC_PCIE_EXCARD_R2D_CP
PCIE_CLK100M_EXCARD_N		NC_PCIE_CLK100M_EXCARDN
PCIE_CLK100M_EXCARD_P		NC_PCIE_CLK100M_EXCARDP
PCIE_PCH_D2R_N<5..8>		NC_PCIE_PCH_D2RN<5..8>
PCIE_PCH_D2R_P<5..8>		NC_PCIE_PCH_D2RP<5..8>
PCIE_PCH_R2D_C_N<5..8>		NC_PCIE_PCH_R2D_CN<5..8>
PCIE_PCH_R2D_C_P<5..8>		NC_PCIE_PCH_R2D_CP<5..8>
PEG_CLK100M_P		NC_PEG_CLK100MP
PEG_CLK100M_N		NC_PEG_CLK100MN
TP_PCH_CLKOUT_DPN		NC_PCH_CLKOUT_DPN
TP_PCH_CLKOUT_DPP		NC_PCH_CLKOUT_DPP

T29BST:N
R0960 0 5% 1/8W MF-LF 805
=PPVIN_SW_T29BST — =PP15V_T29_REG

T29_A_BIAS — C0960 0.01UF 10% 16V X5R-CERM 0201
DP_A_BIAS0 — C0962 0.01UF 10% 16V X5R-CERM 0201
DP_A_BIAS2 — C0964 0.01UF 10% 16V X5R-CERM 0201

T29_A_BIAS_R2DP1
T29_A_BIAS_R2DN0
T29_A_BIAS — R0970 51 1/20W — T29_A_BIAS_R2DP0 (VOLTAGE=3.3V) — C0970 0.01UF 10% 16V X5R-CERM 0201
R0971 51 1/20W — T29_A_BIAS_R2DN1 (VOLTAGE=3.3V) — C0971 0.01UF 10% 16V X5R-CERM 0201
R0972 51 1/20W — T29_A_BIAS_D2RP1 (VOLTAGE=3.3V) — C0972 0.01UF 10% 16V X5R-CERM 0201
R0973 51 1/20W — T29_A_BIAS_D2RN1 (VOLTAGE=3.3V) — C0973 0.01UF 10% 16V X5R-CERM 0201

TBT JTAG

JTAG_ISP_TCK (IN)		JTAG_TBT_TCK (OUT)
JTAG_ISP_TDI (IN)		JTAG_TBT_TDI (OUT)
JTAG_ISP_TDO (OUT)		JTAG_TBT_TDO (IN)

T29 DP Ports

DPB_IG_HPD		DP_T29SNK0_HPD
TP_DP_IG_C_MLP<3..0>		DP_T29SNK0_ML_C_P<3..0>
TP_DP_IG_C_MLN<3..0>		DP_T29SNK0_ML_C_N<3..0>
DPB_IG_AUX_CH_P		DP_T29SNK0_AUXCH_C_P
DPB_IG_AUX_CH_N		DP_T29SNK0_AUXCH_C_N
TP_DP_IG_D_HPD		DP_T29SNK1_HPD
TP_DP_IG_D_MLP<3..0>		DP_T29SNK1_ML_C_P<3..0>
TP_DP_IG_D_MLN<3..0>		DP_T29SNK1_ML_C_N<3..0>
TP_DP_IG_D_AUXP		DP_T29SNK1_AUXCH_C_P
TP_DP_IG_D_AUXN		DP_T29SNK1_AUXCH_C_N
NC_BCM57765_CE_L_MS_INS_L		BCM57765_CE_L_MS_INS_L
TP_LVDS_IG_B_CLKP		LVDS_IG_B_CLK_P
TP_LVDS_IG_B_CLKN		LVDS_IG_B_CLK_N
NC_LVDS_IG_B_DATAP<0..3>		LVDS_IG_B_DATA_P<0..3>
NC_LVDS_IG_B_DATAN<0..3>		LVDS_IG_B_DATA_N<0..3>
NC_LVDS_IG_A_DATAP<3>		LVDS_IG_A_DATA_P<3>
NC_LVDS_IG_A_DATAN<3>		LVDS_IG_A_DATA_N<3>
LVDS_DDC_CLK		LVDS_IG_DDC_CLK
LVDS_DDC_DATA		LVDS_IG_DDC_DATA
LCD_BKLT_PWM		LVDS_IG_BKL_PWM
LCD_IG_PWR_EN		LVDS_IG_PANEL_PWR
LCD_BKLT_EN		LVDS_IG_BKL_ON

PCIE_T29_R2D_C_P<3..0>		R2D_C_P<12..15>
PCIE_T29_R2D_C_N<3..0>		R2D_C_N<12..15>
PCIE_T29_D2R_P<3..0>		=PEG_D2R_P<12..15>
PCIE_T29_D2R_N<3..0>		=PEG_D2R_N<12..15>

=PP3V3_S0_DP_DDC
R0920 2.2K 5% 1/16W MF-LF 402
R0921 2.2K 5% 1/16W MF-LF 402
R0922 2.2K 5% 1/16W MF-LF 402
R0923 2.2K 5% 1/16W MF-LF 402

TP_DP_IG_C_CTRL_CLK		DPB_IG_DDC_CLK
TP_DP_IG_C_CTRL_DATA		DPB_IG_DDC_DATA
TP_DP_IG_D_CTRL_CLK		DP_IG_D_CTRL_CLK
TP_DP_IG_D_CTRL_DATA		DP_IG_D_CTRL_DATA

=PP3V3_S0_DP_DDC
R0924 2.2K 5% 1/16W MF-LF 402
R0925 2.2K 5% 1/16W MF-LF 402

DP_EXTA_DDC_CLK		DPA_IG_DDC_CLK
DP_EXTA_DDC_DATA		DPA_IG_DDC_DATA
DP_EXTA_HPD		DPA_IG_HPD

R0908 100K 5% 1/16W MF-LF 402

R0910 0 5% 1/16W MF-LF 402
PPBUS_SW_LCDBKLT_PWR — PPBUS_SW_BKL (MIN_LINE_WIDTH=0.5 MM, MIN_NECK_WIDTH=0.375 MM, VOLTAGE=12.6V, MAKE_BASE=TRUE) — =PPBUS_SW_BKL

NC_CPU_VCCIO_SEL — CPU_VCCIO_SEL

USB Signals

NC_USB3_EXTD_TXN		USB3_EXTD_TX_N
NC_USB3_EXTD_TXP		USB3_EXTD_TX_P
NC_USB3_EXTD_RXN		USB3_EXTD_RX_N
NC_USB3_EXTD_RXP		USB3_EXTD_RX_P
USB_BT_N		USBHUB_DN1_N
USB_BT_P		USBHUB_DN1_P
USB_TPAD_N		USBHUB_DN3_N
USB_TPAD_P		USBHUB_DN3_P
USB_IR_N		USBHUB_DN2_N
USB_IR_P		USBHUB_DN2_P
USB_SMC_N		NC_USB_SMCN
USB_SMC_P		NC_USB_SMCP
NC_USB_EXTD_EHCIN		USB_EXTD_EHCI_N
NC_USB_EXTD_EHCIP		USB_EXTD_EHCI_P
NC_USB_EXTCN		USB_EXTC_N
NC_USB_EXTCP		USB_EXTC_P
NC_USB3_EXTC_TXN		USB3_EXTC_TX_N
NC_USB3_EXTC_TXP		USB3_EXTC_TX_P
NC_USB3_EXTC_RXN		USB3_EXTC_RX_N
NC_USB3_EXTC_RXP		USB3_EXTC_RX_P
NC_USB_EXTD_XHCIN		USB_EXTD_XHCI_N
NC_USB_EXTD_XHCIP		USB_EXTD_XHCI_P
TP_CPU_THERMDP		CPU_THERMD_P
TP_CPU_THERMDN		CPU_THERMD_N
TP_CPU_VTT_SELECT		CPU_VTTSELECT

Unused eDP CLK

DPLL_REF_CLK_P		DPLL_REF_CLKP
DPLL_REF_CLK_N		DPLL_REF_CLKN

=PP1V05_S0_CPU_VCCPQE — R0940 1K 5% 1/16W MF-LF 402 — R0941 1K 5% 1/16W MF-LF 402

PM_SLP_S3_L — =TBT_S0_EN

Unused T29 Ports

T29_D2R_P<2..3> (OUT)		NC_T29_D2RP<2..3>
T29_D2R_N<2..3> (OUT)		NC_T29_D2RN<2..3>
T29_R2D_C_P<2..3> (IN)		NC_T29_R2D_CP<2..3>
T29_R2D_C_N<2..3> (IN)		NC_T29_R2D_CN<2..3>
T29_LSEO<2> (IN)		T29_LSOE<2> (OUT)
T29_LSEO<3> (IN)		T29_LSOE<3> (OUT)

Unused PGOOD signal

TP_P1V5S3RS0_RAMP_DONE		P1V5S3RS0_RAMP_DONE (IN)
TP_DDRREG_PGOOD		DDRREG_PGOOD (IN)

Digital Ground

GND (MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.2MM, VOLTAGE=0V)

SYNC_MASTER=K90I_MLB — SYNC_DATE=02/15/2011
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Signal Aliases

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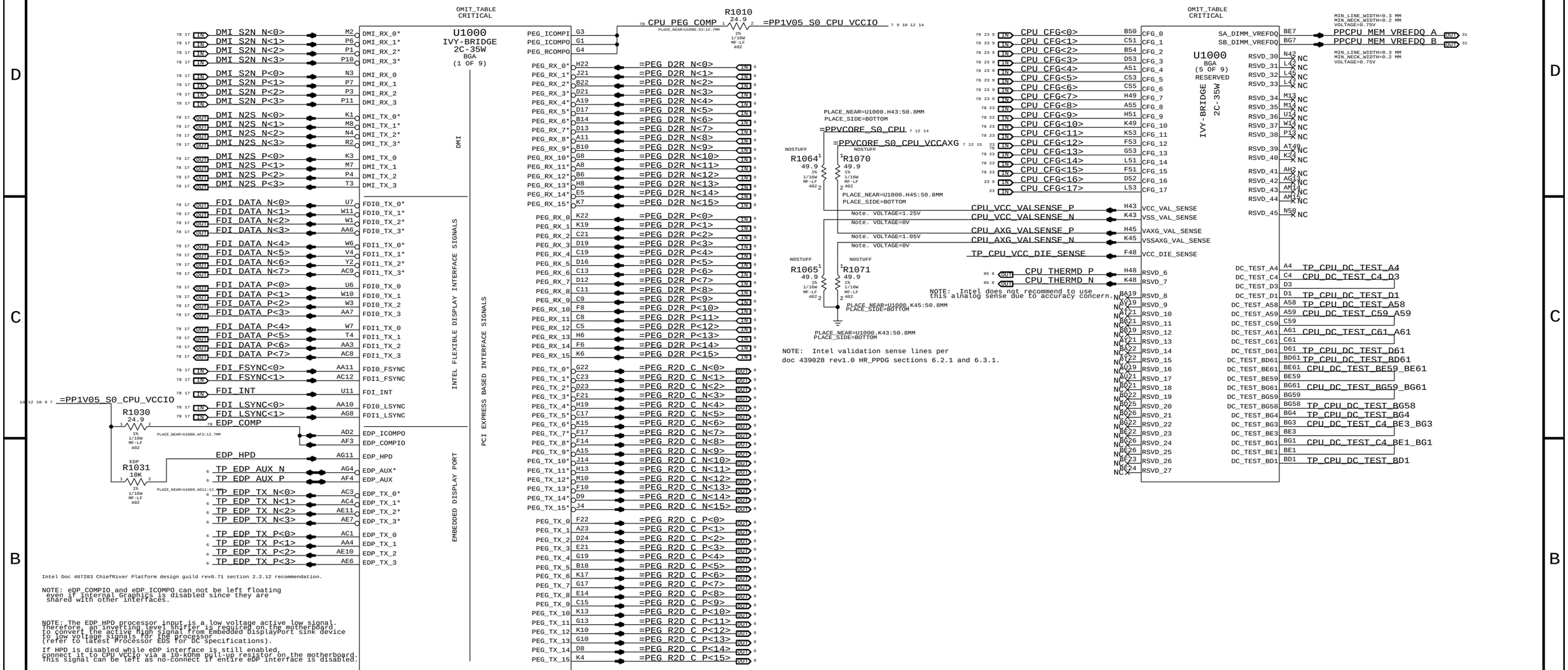
NOTE: Intel provides an internal pull-up OF 5-15k to VCCIO on all CFG signals.



Intel Doc 467283 ChiefRiver Platform design guild rev0.71 section 2.2.12 recommendation.

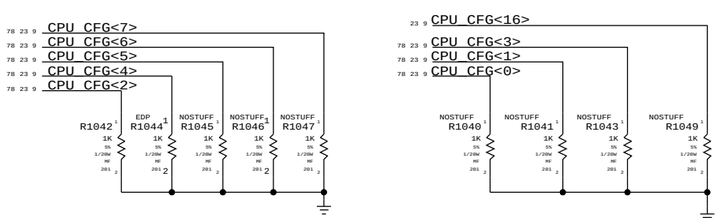
NOTE: eDP_COMPIO and eDP_ICOMPO can not be left floating even if internal Graphics is disabled since they are shared with other interfaces.

NOTE: The EDP_HPD processor input is a low voltage active low signal. Therefore, an inverting level shifter is required on the motherboard to convert the active high signal from Embedded DisplayPort sink device to low voltage signals for the processor (refer to latest Processor EDS for DC specifications).

If HPD is disabled while eDP interface is still enabled, connect it to CPU_VCCIO via a 10-kOhm pull-up resistor on the motherboard. This signal can be left as no-connect if entire eDP interface is disabled.

NOTE: Intel does not recommend to use this alnalog sense due to accuracy concern.

NOTE: Intel validation sense lines per doc 439028 rev1.0 HR_PPDG sections 6.2.1 and 6.3.1.



These can be Placed close to J2500 and Only for debug access

FOR IVYBRIDGE PROCESSOR

CFG [7] :PEG DEFER TRAINING	1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB	0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION	11 = 1 X16 (DEFAULT) 10 = 2 X8	01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE	1 = DISABLED	0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL	1 = NORMAL OPERATION	0 = LANES REVERSED

SYNC MASTER=MASTER SYNC DATE=02/15/2013

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CPU DMI/PEG/FDI/RSVD

Apple Inc.

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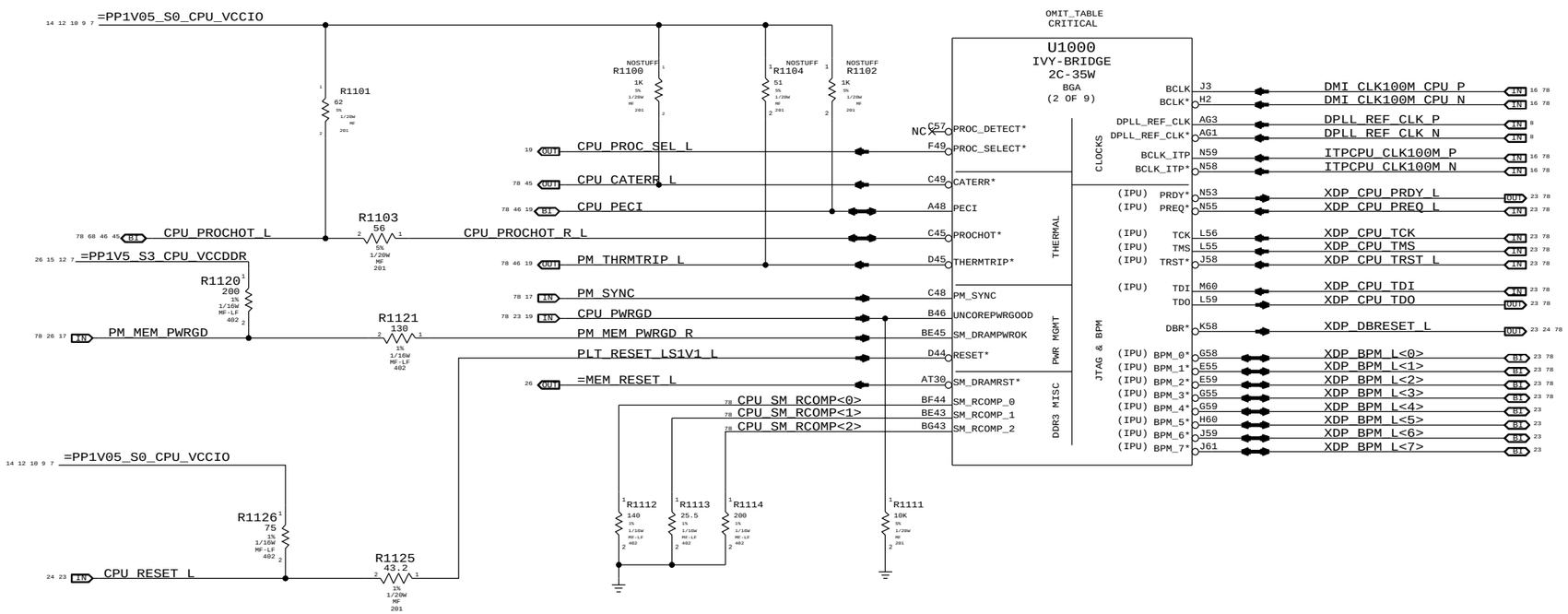

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OMIT_TABLE
CRITICAL

U1000
BGA
(3 OF 9)
IVY-BRIDGE
2C-35W
MEMORY CHANNEL A

MEM_A_DQ<0>	AG6	SA_DQ_0	
MEM_A_DQ<1>	AJ6	SA_DQ_1	
MEM_A_DQ<2>	AP11	SA_DQ_2	
MEM_A_DQ<3>	AL6	SA_DQ_3	
MEM_A_DQ<4>	AJ10	SA_DQ_4	
MEM_A_DQ<5>	AJ8	SA_DQ_5	
MEM_A_DQ<6>	AL8	SA_DQ_6	
MEM_A_DQ<7>	AL7	SA_DQ_7	
MEM_A_DQ<8>	AR11	SA_DQ_8	
MEM_A_DQ<9>	AP6	SA_DQ_9	
MEM_A_DQ<10>	AU6	SA_DQ_10	
MEM_A_DQ<11>	AV9	SA_DQ_11	
MEM_A_DQ<12>	AR6	SA_DQ_12	
MEM_A_DQ<13>	AP8	SA_DQ_13	
MEM_A_DQ<14>	AT13	SA_DQ_14	
MEM_A_DQ<15>	AU13	SA_DQ_15	
MEM_A_DQ<16>	BC7	SA_DQ_16	
MEM_A_DQ<17>	BB7	SA_DQ_17	
MEM_A_DQ<18>	BA13	SA_DQ_18	
MEM_A_DQ<19>	BB11	SA_DQ_19	
MEM_A_DQ<20>	BA7	SA_DQ_20	
MEM_A_DQ<21>	BA9	SA_DQ_21	
MEM_A_DQ<22>	BB9	SA_DQ_22	
MEM_A_DQ<23>	AY13	SA_DQ_23	
MEM_A_DQ<24>	AV14	SA_DQ_24	
MEM_A_DQ<25>	AR14	SA_DQ_25	
MEM_A_DQ<26>	AY17	SA_DQ_26	
MEM_A_DQ<27>	AR19	SA_DQ_27	
MEM_A_DQ<28>	BA14	SA_DQ_28	
MEM_A_DQ<29>	AU14	SA_DQ_29	
MEM_A_DQ<30>	BB14	SA_DQ_30	
MEM_A_DQ<31>	BB17	SA_DQ_31	
MEM_A_DQ<32>	BA45	SA_DQ_32	
MEM_A_DQ<33>	AR43	SA_DQ_33	
MEM_A_DQ<34>	AW48	SA_DQ_34	
MEM_A_DQ<35>	BC48	SA_DQ_35	
MEM_A_DQ<36>	BC45	SA_DQ_36	
MEM_A_DQ<37>	AR45	SA_DQ_37	
MEM_A_DQ<38>	AT48	SA_DQ_38	
MEM_A_DQ<39>	AY48	SA_DQ_39	
MEM_A_DQ<40>	BA49	SA_DQ_40	
MEM_A_DQ<41>	AV49	SA_DQ_41	
MEM_A_DQ<42>	BB51	SA_DQ_42	
MEM_A_DQ<43>	AY53	SA_DQ_43	
MEM_A_DQ<44>	BB49	SA_DQ_44	
MEM_A_DQ<45>	AU49	SA_DQ_45	
MEM_A_DQ<46>	BA53	SA_DQ_46	
MEM_A_DQ<47>	BB55	SA_DQ_47	
MEM_A_DQ<48>	BA55	SA_DQ_48	
MEM_A_DQ<49>	AV56	SA_DQ_49	
MEM_A_DQ<50>	AP50	SA_DQ_50	
MEM_A_DQ<51>	AP53	SA_DQ_51	
MEM_A_DQ<52>	AV54	SA_DQ_52	
MEM_A_DQ<53>	AT54	SA_DQ_53	
MEM_A_DQ<54>	AP56	SA_DQ_54	
MEM_A_DQ<55>	AP52	SA_DQ_55	
MEM_A_DQ<56>	AN57	SA_DQ_56	
MEM_A_DQ<57>	AN53	SA_DQ_57	
MEM_A_DQ<58>	AG56	SA_DQ_58	
MEM_A_DQ<59>	AG53	SA_DQ_59	
MEM_A_DQ<60>	AN55	SA_DQ_60	
MEM_A_DQ<61>	AN52	SA_DQ_61	
MEM_A_DQ<62>	AG55	SA_DQ_62	
MEM_A_DQ<63>	AK56	SA_DQ_63	
MEM_A_BA<0>	BD37	SA_BS_0	
MEM_A_BA<1>	BF36	SA_BS_1	
MEM_A_BA<2>	BA28	SA_BS_2	
MEM_A_CAS_L	BE39	SA_CAS*	
MEM_A_RAS_L	BD39	SA_RAS*	
MEM_A_WE_L	AT41	SA_WE*	
	AU36	SA_CK_0	MEM_A_CLK_P<0>
	AV36	SA_CK_0*	MEM_A_CLK_N<0>
	AY26	SA_CKE_0	MEM_A_CKE<0>
	AT40	SA_CK_1	MEM_A_CLK_P<1>
	AU40	SA_CK_1*	MEM_A_CLK_N<1>
	BB26	SA_CKE_1	MEM_A_CKE<1>
	BB40	SA_CS_0*	MEM_A_CS_L<0>
	BC41	SA_CS_1*	MEM_A_CS_L<1>
	AY40	SA_ODT_0	MEM_A_ODT<0>
	BA41	SA_ODT_1	MEM_A_ODT<1>
	AL11	SA_DQS_0*	MEM_A_DQS_N<0>
	AR8	SA_DQS_1*	MEM_A_DQS_N<1>
	AV11	SA_DQS_2*	MEM_A_DQS_N<2>
	AT17	SA_DQS_3*	MEM_A_DQS_N<3>
	AV45	SA_DQS_4*	MEM_A_DQS_N<4>
	AY51	SA_DQS_5*	MEM_A_DQS_N<5>
	AT55	SA_DQS_6*	MEM_A_DQS_N<6>
	AK55	SA_DQS_7*	MEM_A_DQS_N<7>
	AJ11	SA_DQS_0	MEM_A_DQS_P<0>
	AR10	SA_DQS_1	MEM_A_DQS_P<1>
	AY11	SA_DQS_2	MEM_A_DQS_P<2>
	AU17	SA_DQS_3	MEM_A_DQS_P<3>
	AW45	SA_DQS_4	MEM_A_DQS_P<4>
	AV51	SA_DQS_5	MEM_A_DQS_P<5>
	AT56	SA_DQS_6	MEM_A_DQS_P<6>
	AK54	SA_DQS_7	MEM_A_DQS_P<7>
	BG35	SA_MA_0	MEM_A_A<0>
	BB34	SA_MA_1	MEM_A_A<1>
	BE35	SA_MA_2	MEM_A_A<2>
	BD35	SA_MA_3	MEM_A_A<3>
	AT34	SA_MA_4	MEM_A_A<4>
	AU34	SA_MA_5	MEM_A_A<5>
	BB32	SA_MA_6	MEM_A_A<6>
	AT32	SA_MA_7	MEM_A_A<7>
	AY32	SA_MA_8	MEM_A_A<8>
	AV32	SA_MA_9	MEM_A_A<9>
	BE37	SA_MA_10	MEM_A_A<10>
	BA30	SA_MA_11	MEM_A_A<11>
	BC30	SA_MA_12	MEM_A_A<12>
	AW41	SA_MA_13	MEM_A_A<13>
	AY28	SA_MA_14	MEM_A_A<14>
	AU26	SA_MA_15	MEM_A_A<15>

OMIT_TABLE
CRITICAL

U1000
BGA
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IVY-BRIDGE
2C-35W
MEMORY CHANNEL B

MEM_B_DQ<0>	AL4	SB_DQ_0	
MEM_B_DQ<1>	AL1	SB_DQ_1	
MEM_B_DQ<2>	AN3	SB_DQ_2	
MEM_B_DQ<3>	AR4	SB_DQ_3	
MEM_B_DQ<4>	AK4	SB_DQ_4	
MEM_B_DQ<5>	AK3	SB_DQ_5	
MEM_B_DQ<6>	AN4	SB_DQ_6	
MEM_B_DQ<7>	AR1	SB_DQ_7	
MEM_B_DQ<8>	AU4	SB_DQ_8	
MEM_B_DQ<9>	AT2	SB_DQ_9	
MEM_B_DQ<10>	AV4	SB_DQ_10	
MEM_B_DQ<11>	BA4	SB_DQ_11	
MEM_B_DQ<12>	AU3	SB_DQ_12	
MEM_B_DQ<13>	AR3	SB_DQ_13	
MEM_B_DQ<14>	AY2	SB_DQ_14	
MEM_B_DQ<15>	BA3	SB_DQ_15	
MEM_B_DQ<16>	BE9	SB_DQ_16	
MEM_B_DQ<17>	BD9	SB_DQ_17	
MEM_B_DQ<18>	BD13	SB_DQ_18	
MEM_B_DQ<19>	BF12	SB_DQ_19	
MEM_B_DQ<20>	BF8	SB_DQ_20	
MEM_B_DQ<21>	BD10	SB_DQ_21	
MEM_B_DQ<22>	BD14	SB_DQ_22	
MEM_B_DQ<23>	BE13	SB_DQ_23	
MEM_B_DQ<24>	BF16	SB_DQ_24	
MEM_B_DQ<25>	BE17	SB_DQ_25	
MEM_B_DQ<26>	BE18	SB_DQ_26	
MEM_B_DQ<27>	BE21	SB_DQ_27	
MEM_B_DQ<28>	BE14	SB_DQ_28	
MEM_B_DQ<29>	BG14	SB_DQ_29	
MEM_B_DQ<30>	BG18	SB_DQ_30	
MEM_B_DQ<31>	BF19	SB_DQ_31	
MEM_B_DQ<32>	BD50	SB_DQ_32	
MEM_B_DQ<33>	BF48	SB_DQ_33	
MEM_B_DQ<34>	BD53	SB_DQ_34	
MEM_B_DQ<35>	BF52	SB_DQ_35	
MEM_B_DQ<36>	BD49	SB_DQ_36	
MEM_B_DQ<37>	BE49	SB_DQ_37	
MEM_B_DQ<38>	BD54	SB_DQ_38	
MEM_B_DQ<39>	BE53	SB_DQ_39	
MEM_B_DQ<40>	BF56	SB_DQ_40	
MEM_B_DQ<41>	BE57	SB_DQ_41	
MEM_B_DQ<42>	BC59	SB_DQ_42	
MEM_B_DQ<43>	AY60	SB_DQ_43	
MEM_B_DQ<44>	BE54	SB_DQ_44	
MEM_B_DQ<45>	BG54	SB_DQ_45	
MEM_B_DQ<46>	BA58	SB_DQ_46	
MEM_B_DQ<47>	AW59	SB_DQ_47	
MEM_B_DQ<48>	AW58	SB_DQ_48	
MEM_B_DQ<49>	AU58	SB_DQ_49	
MEM_B_DQ<50>	AN61	SB_DQ_50	
MEM_B_DQ<51>	AN59	SB_DQ_51	
MEM_B_DQ<52>	AU59	SB_DQ_52	
MEM_B_DQ<53>	AU61	SB_DQ_53	
MEM_B_DQ<54>	AN58	SB_DQ_54	
MEM_B_DQ<55>	AR58	SB_DQ_55	
MEM_B_DQ<56>	AK58	SB_DQ_56	
MEM_B_DQ<57>	AL58	SB_DQ_57	
MEM_B_DQ<58>	AG58	SB_DQ_58	
MEM_B_DQ<59>	AG59	SB_DQ_59	
MEM_B_DQ<60>	AM60	SB_DQ_60	
MEM_B_DQ<61>	AL59	SB_DQ_61	
MEM_B_DQ<62>	AF61	SB_DQ_62	
MEM_B_DQ<63>	AH60	SB_DQ_63	
MEM_B_BA<0>	BG39	SB_BS_0	
MEM_B_BA<1>	BD42	SB_BS_1	
MEM_B_BA<2>	AT22	SB_BS_2	
MEM_B_CAS_L	AV43	SB_CAS*	
MEM_B_RAS_L	BF40	SB_RAS*	
MEM_B_WE_L	BD45	SB_WE*	
	BA34	SB_CK_0	MEM_B_CLK_P<0>
	AY34	SB_CK_0*	MEM_B_CLK_N<0>
	AR22	SB_CKE_0	MEM_B_CKE<0>
	BA36	SB_CK_1	MEM_B_CLK_P<1>
	BB36	SB_CK_1*	MEM_B_CLK_N<1>
	BF27	SB_CKE_1	MEM_B_CKE<1>
	BE41	SB_CS_0*	MEM_B_CS_L<0>
	BE47	SB_CS_1*	MEM_B_CS_L<1>
	AT43	SB_ODT_0	MEM_B_ODT<0>
	BG47	SB_ODT_1	MEM_B_ODT<1>
	AL3	SB_DQS_0*	MEM_B_DQS_N<0>
	AV3	SB_DQS_1*	MEM_B_DQS_N<1>
	BG11	SB_DQS_2*	MEM_B_DQS_N<2>
	BD17	SB_DQS_3*	MEM_B_DQS_N<3>
	BG51	SB_DQS_4*	MEM_B_DQS_N<4>
	BA59	SB_DQS_5*	MEM_B_DQS_N<5>
	AT60	SB_DQS_6*	MEM_B_DQS_N<6>
	AK59	SB_DQS_7*	MEM_B_DQS_N<7>
	AM2	SB_DQS_0	MEM_B_DQS_P<0>
	AV1	SB_DQS_1	MEM_B_DQS_P<1>
	BE11	SB_DQS_2	MEM_B_DQS_P<2>
	BD18	SB_DQS_3	MEM_B_DQS_P<3>
	BE51	SB_DQS_4	MEM_B_DQS_P<4>
	BA61	SB_DQS_5	MEM_B_DQS_P<5>
	AR59	SB_DQS_6	MEM_B_DQS_P<6>
	AK61	SB_DQS_7	MEM_B_DQS_P<7>
	BF32	SB_MA_0	MEM_B_A<0>
	BE33	SB_MA_1	MEM_B_A<1>
	BD33	SB_MA_2	MEM_B_A<2>
	AU30	SB_MA_3	MEM_B_A<3>
	BD30	SB_MA_4	MEM_B_A<4>
	AV30	SB_MA_5	MEM_B_A<5>
	BG30	SB_MA_6	MEM_B_A<6>
	BD29	SB_MA_7	MEM_B_A<7>
	BE30	SB_MA_8	MEM_B_A<8>
	BE28	SB_MA_9	MEM_B_A<9>
	BD43	SB_MA_10	MEM_B_A<10>
	AT28	SB_MA_11	MEM_B_A<11>
	AV28	SB_MA_12	MEM_B_A<12>
	BD46	SB_MA_13	MEM_B_A<13>
	AT26	SB_MA_14	MEM_B_A<14>
	AU22	SB_MA_15	MEM_B_A<15>

SYNC_MASTER=MASTER SYNC_DATE=02/15/2011

PAGE TITLE
CPU DDR3 INTERFACES

Apple Inc.

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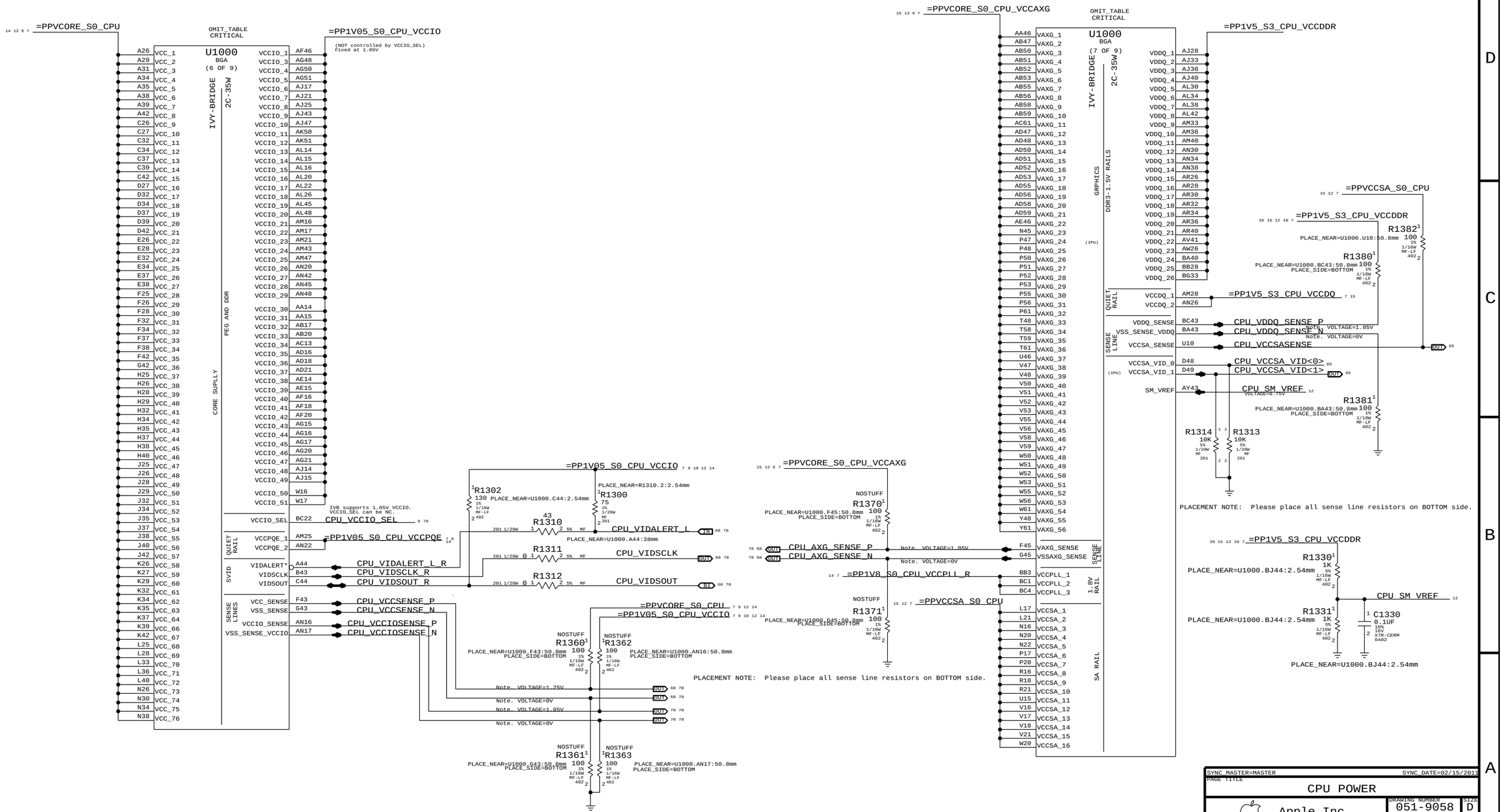

SYNC MASTER=MASTER SYNC DATE=02/15/2013

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CPU POWER

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

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OMIT_TABLE
CRITICAL

U1000
BGA
(9 OF 9)
IVY-BRIDGE
2C-35W

BG13	VSS	VSS	M11
BG17	VSS	VSS	M15
BG21	VSS	VSS	M58
BG24	VSS	VSS	N1
BG28	VSS	VSS	N17
BG37	VSS	VSS	N21
BG41	VSS	VSS	N25
BG45	VSS	VSS	N28
BG49	VSS	VSS	N33
BG53	VSS	VSS	N36
C29	VSS	VSS	N40
C35	VSS	VSS	N43
C40	VSS	VSS	N47
D4	VSS	VSS	N48
D6	VSS	VSS	N51
D10	VSS	VSS	N52
D14	VSS	VSS	N56
D18	VSS	VSS	N61
D22	VSS	VSS	P9
D26	VSS	VSS	P14
D29	VSS	VSS	P16
D35	VSS	VSS	P18
D40	VSS	VSS	P21
D43	VSS	VSS	P58
D46	VSS	VSS	P59
D50	VSS	VSS	R4
D54	VSS	VSS	R17
D58	VSS	VSS	R20
E3	VSS	VSS	R46
E25	VSS	VSS	T1
E29	VSS	VSS	T47
E35	VSS	VSS	T50
E40	VSS	VSS	T51
F13	VSS	VSS	T52
F15	VSS	VSS	T53
F19	VSS	VSS	T55
F29	VSS	VSS	T56
F35	VSS	VSS	U8
F40	VSS	VSS	U13
F55	VSS	VSS	V20
G6	VSS	VSS	V61
G48	VSS	VSS	W8
G51	VSS	VSS	W13
G61	VSS	VSS	W15
H4	VSS	VSS	W18
H10	VSS	VSS	W21
H14	VSS	VSS	W46
H17	VSS	VSS	Y4
H21	VSS	VSS	Y47
H53	VSS	VSS	Y58
H58	VSS	VSS	Y59
J1	VSS		
J49	VSS		
J55	VSS		
K8	VSS		
K11	VSS		
K21	VSS	VSS_NCTF	A5
K51	VSS	VSS_NCTF	A57
L16	VSS	VSS_NCTF	BC61
L20	VSS	VSS_NCTF	BD3
L22	VSS	VSS_NCTF	BD59
L26	VSS	VSS_NCTF	BE4
L30	VSS	VSS_NCTF	BE58
L34	VSS	VSS_NCTF	BG5
L38	VSS	VSS_NCTF	BG57
L43	VSS	VSS_NCTF	C3
L48	VSS	VSS_NCTF	C58
L61	VSS	VSS_NCTF	D59
M4	VSS	VSS_NCTF	E1
M6	VSS	VSS_NCTF	E61

OMIT_TABLE
CRITICAL

U1000
BGA
(8 OF 9)
IVY-BRIDGE
2C-35W

A9	VSS	VSS	AM34
A13	VSS	VSS	AM38
A17	VSS	VSS	AM42
A21	VSS	VSS	AM45
A25	VSS	VSS	AM48
A28	VSS	VSS	AM58
A33	VSS	VSS	AN1
A37	VSS	VSS	AN21
A40	VSS	VSS	AN25
A45	VSS	VSS	AN28
A49	VSS	VSS	AN33
A53	VSS	VSS	AN36
AA1	VSS	VSS	AN40
AA8	VSS	VSS	AN43
AA13	VSS	VSS	AN47
AA50	VSS	VSS	AN50
AA51	VSS	VSS	AN54
AA52	VSS	VSS	AP7
AA53	VSS	VSS	AP10
AA55	VSS	VSS	AP51
AA56	VSS	VSS	AP55
AB16	VSS	VSS	AR7
AB18	VSS	VSS	AR13
AB21	VSS	VSS	AR17
AB48	VSS	VSS	AR21
AB61	VSS	VSS	AR41
AC6	VSS	VSS	AR48
AC10	VSS	VSS	AR61
AC14	VSS	VSS	AT4
AC46	VSS	VSS	AT14
AD4	VSS	VSS	AT19
AD17	VSS	VSS	AT36
AD20	VSS	VSS	AT45
AD61	VSS	VSS	AT52
AE8	VSS	VSS	AT58
AE13	VSS	VSS	AU1
AF1	VSS	VSS	AU7
AF17	VSS	VSS	AU11
AF21	VSS	VSS	AU28
AF47	VSS	VSS	AU32
AF48	VSS	VSS	AU51
AF50	VSS	VSS	AV17
AF51	VSS	VSS	AV21
AF52	VSS	VSS	AV22
AF53	VSS	VSS	AV34
AF55	VSS	VSS	AV40
AF56	VSS	VSS	AV48
AF58	VSS	VSS	AV55
AF59	VSS	VSS	AW7
AG7	VSS	VSS	AW13
AG10	VSS	VSS	AW43
AG14	VSS	VSS	AW61
AG18	VSS	VSS	AY4
AG47	VSS	VSS	AY9
AG52	VSS	VSS	AY14
AG61	VSS	VSS	AY19
AH4	VSS	VSS	AY30
AH58	VSS	VSS	AY36
AJ7	VSS	VSS	AY41
AJ13	VSS	VSS	AY45
AJ16	VSS	VSS	AY49
AJ20	VSS	VSS	AY55
AJ22	VSS	VSS	AY58
AJ26	VSS	VSS	BA1
AJ30	VSS	VSS	BA11
AJ34	VSS	VSS	BA17
AJ38	VSS	VSS	BA21
AJ42	VSS	VSS	BA26
AJ45	VSS	VSS	BA32
AJ48	VSS	VSS	BA48
AK1	VSS	VSS	BA51
AK52	VSS	VSS	BB53
AL10	VSS	VSS	BC5
AL13	VSS	VSS	BC13
AL17	VSS	VSS	BC57
AL21	VSS	VSS	BD8
AL25	VSS	VSS	BD12
AL28	VSS	VSS	BD16
AL33	VSS	VSS	BD19
AL36	VSS	VSS	BD23
AL40	VSS	VSS	BD27
AL43	VSS	VSS	BD32
AL47	VSS	VSS	BD36
AL61	VSS	VSS	BD40
AM4	VSS	VSS	BD44
AM13	VSS	VSS	BD48
AM20	VSS	VSS	BD52
AM22	VSS	VSS	BD56
AM26	VSS	VSS	BE5
AM30	VSS	VSS	BG9

SYNC MASTER=MASTER SYNC DATE=02/15/2013

PAGE TITLE
CPU GROUNDS

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

REVISION 6.0.0

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF

12 9 7 =PPVCORE_S0_CPU

C1600 C1604 C1606 C1607 C1608 C1609 C1610 C1612 C1613 C1615 C1617 C1623 C1624
2.2UF 20% 4V X5R 402

C1625 C1627 C1628 C1631 C1632 C1635 C1637 C1638 C1639 C1640 C1641 C1642 C1643 C1644 C1645 C1647 C1648
2.2UF 20% 4V X5R 402

C1650 C1651 C1652 C1653 C1654
2.2UF 20% 4V X5R 402

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

C1655 C1656 C1657 C1658 C1659 C1660 C1661 C1662 C1663 C1664 C1665 C1666
22UF 20% 6.3V X5R-CERM-1 603

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

C1667 C1668 C1669 C1670 C1671 C1672 C1673 C1674 C1675 C1676 C1677 C1678 C1679
22UF 20% 6.3V X5R-CERM-1 603

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

C1680 C1681 C1682 C1683
470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	16	CAP,CER,X5R,22uF,20%,6.3V,0603,SAMSUNG	C1655,C1660,C1661,C1664,C1666,C1667,C1670,C1677,C1678,C1679,C1657,C1672,C1658,C1669,C1668,C1656	CRITICAL	

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

12 10 9 7 =PP1V05_S0_CPU_VCCIO

C1684 C1685 C1686 C1687 C1688 C1689 C1690 C1691 C1692 C1693 C1694 C1695 C1696
1UF 10% 10V X5R 402

C1697 C1698 C1699 C169A C169B C169C C169D C169E C169F C161A C161B C161C C161D
1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E C161F C162A C162B C162C C162D C162E C167A C167B C167C
10UF 20% 6.3V X5R 603 / CERM-X5R 0402-1

C167D C167E C167G C167H C167J
330UF 20% 2.5V TANT CASE-B2-SM1

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603 — =PP1V05_S0_CPU_VCCPQE 7 8 12

C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):
Place near U1000 on top side

7 =PP1V8_S0_CPU_VCCPLL — R1600 0 5% 1/16W MF-LF 402 — =PP1V8_S0_CPU_VCCPLL_R 7 12

PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA

C160X C160Y 1UF 10% 10V X5R 402

PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

PLACE_NEAR=U1000.BC1:5mm

C160Z 330UF-0.0060OHM 20% 2V POLY CASE-D2-SM

CPU VCCPLL Low pass filter

SYNC_MASTER=JACK_J30 SYNC_DATE=09/27/2013

PAGE TITLE: CPU DECOUPLING-I

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

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VAXG DECOUPLING

Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

12 9 7 =PPVCORE_S0_CPU_VCCAXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R 402
CRITICAL C1701 1UF 10% 10V X5R 402
CRITICAL C1702 1UF 10% 10V X5R 402
CRITICAL C1703 1UF 10% 10V X5R 402
CRITICAL C1704 1UF 10% 10V X5R 402
CRITICAL C1705 1UF 10% 10V X5R 402
CRITICAL C1706 1UF 10% 10V X5R 402
CRITICAL C1707 1UF 10% 10V X5R 402
CRITICAL C1708 1UF 10% 10V X5R 402
CRITICAL C1709 1UF 10% 10V X5R 402
CRITICAL C1710 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1712 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1713 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1714 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1715 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL OMIT C1717 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1718 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1719 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1720 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1721 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1722 22UF 20% 6.3V X5R-CERM-1 603

PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.

C1723 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1
C1724 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	6	CAP,CER,X5R,22uF,20%,6.3V,0603,SAMSUNG	C1717,C1718,C1719,C1720,C1721,C1722	CRITICAL	

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

26 12 10 7 =PP1V5_S3_CPU_VCCDDR

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603

=PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 6x 1uf, 5x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

12 7 =PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

C1768 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

SYNC_MASTER=MASTER SYNC_DATE=02/15/2011

PAGE TITLE: CPU DECOUPLING-II

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

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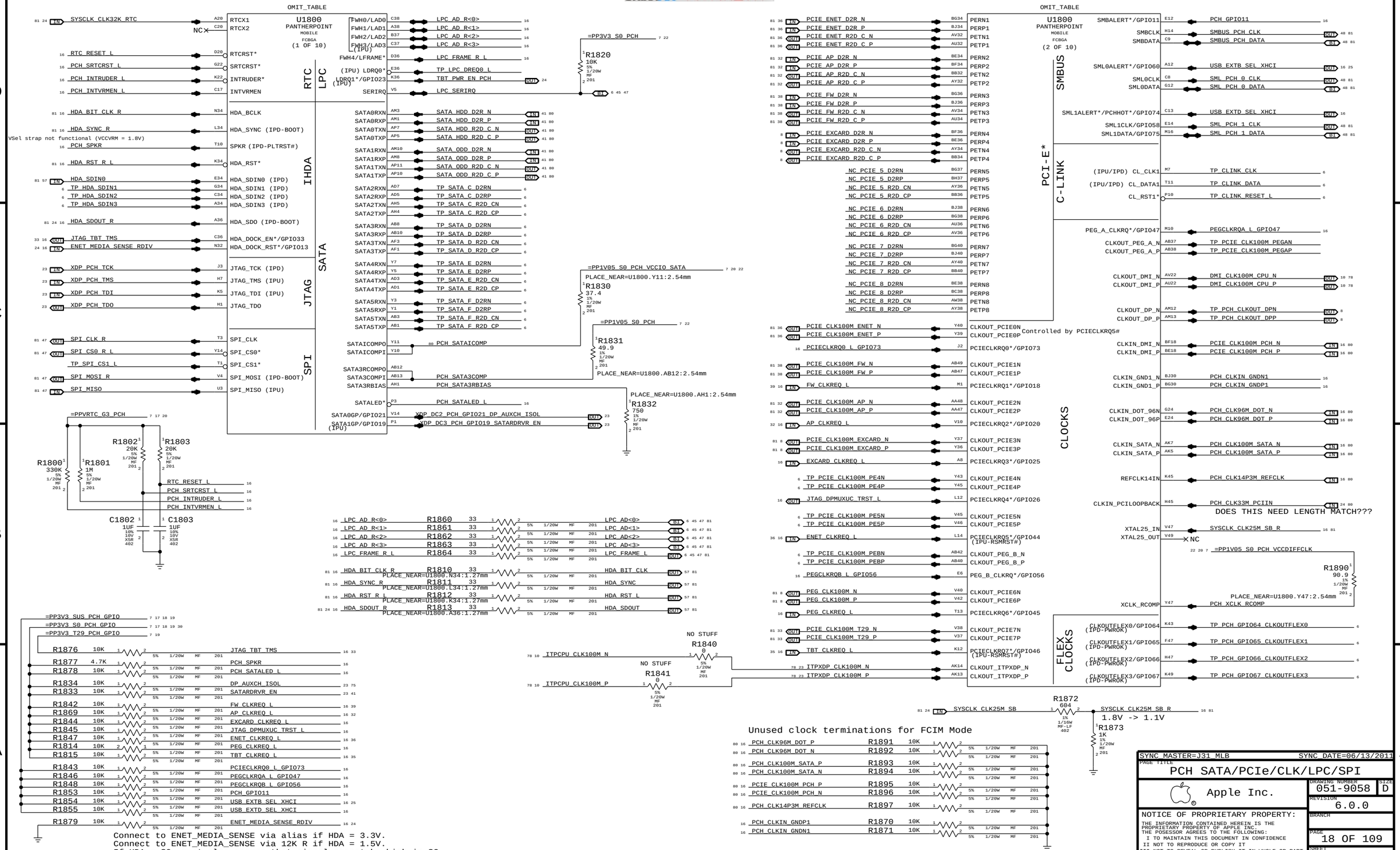

SYNC_MASTER=J31_MLB SYNC_DATE=06/13/2011

PAGE TITLE

PCH SATA/PCIe/CLK/LPC/SPI

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DRAWING NUMBER 051-9058 SIZE D

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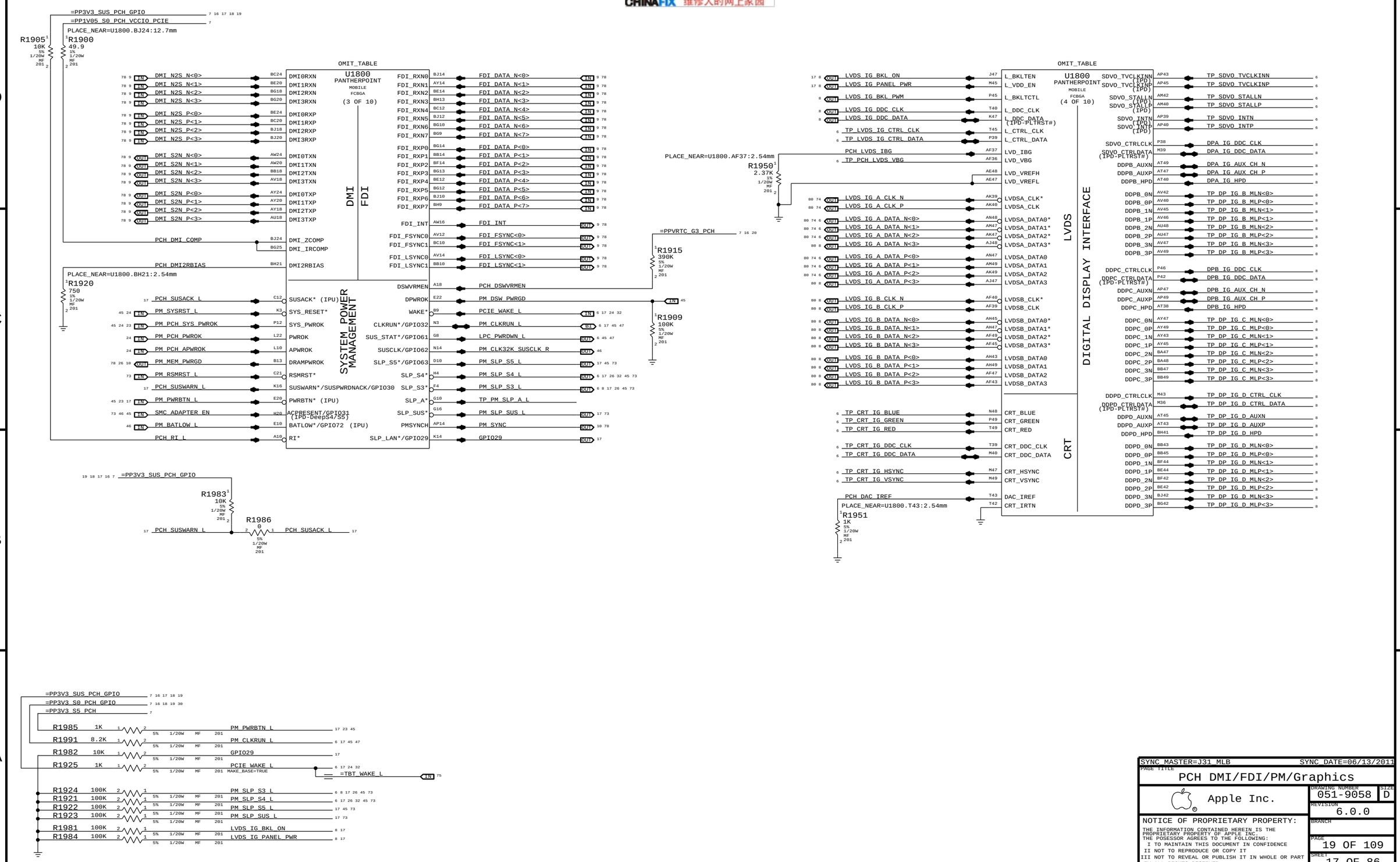
U1800
PANTHERPOINT
MOBILE
FCBGA
(3 OF 10)
DMI
FDI
SYSTEM POWER MANAGEMENT
OMIT_TABLE
=PP3V3_SUS_PCH_GPIO
=PP1V05_S0_PCH_VCCIO_PCIE
PLACE_NEAR=U1800.BJ24:12.7mm
R1905 10K
R1900 49.9
DMI_N2S_N<0>
DMI_N2S_N<1>
DMI_N2S_N<2>
DMI_N2S_N<3>
DMI_N2S_P<0>
DMI_N2S_P<1>
DMI_N2S_P<2>
DMI_N2S_P<3>
DMI_S2N_N<0>
DMI_S2N_N<1>
DMI_S2N_N<2>
DMI_S2N_N<3>
DMI_S2N_P<0>
DMI_S2N_P<1>
DMI_S2N_P<2>
DMI_S2N_P<3>
PCH_DMI_COMP
PCH_DMI2RBIAS
PLACE_NEAR=U1800.BH21:2.54mm
R1920 750
PCH_SUSACK_L
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PM_PCH_APWROK
PM_MEM_PWRGD
PM_RSMRST_L
PCH_SUSWARN_L
PM_PWRBTN_L
SMC_ADAPTER_EN
PM_BATLOW_L
PCH_RI_L
FDI_DATA_N<0>
FDI_DATA_N<1>
FDI_DATA_N<2>
FDI_DATA_N<3>
FDI_DATA_N<4>
FDI_DATA_N<5>
FDI_DATA_N<6>
FDI_DATA_N<7>
FDI_DATA_P<0>
FDI_DATA_P<1>
FDI_DATA_P<2>
FDI_DATA_P<3>
FDI_DATA_P<4>
FDI_DATA_P<5>
FDI_DATA_P<6>
FDI_DATA_P<7>
FDI_INT
FDI_FSYNC<0>
FDI_FSYNC<1>
FDI_LSYNC<0>
FDI_LSYNC<1>
PCH_DSWVRMEN
PM_DSW_PWRGD
PCIE_WAKE_L
PM_CLKRUN_L
LPC_PWRDWN_L
PM_CLK32K_SUSCLK_R
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PM_SLP_A_L
PM_SLP_SUS_L
PM_SYNC
GPIO29
=PPVRTC_G3_PCH
R1915 390K
R1909 100K
=PP3V3_SUS_PCH_GPIO
R1983 10K
R1986 0
PCH_SUSWARN_L
PCH_SUSACK_L
=PP3V3_S0_PCH_GPIO
=PP3V3_S5_PCH
R1985 1K PM_PWRBTN_L
R1991 8.2K PM_CLKRUN_L
R1982 10K GPIO29
R1925 1K PCIE_WAKE_L
=TBT_WAKE_L
R1924 100K PM_SLP_S3_L
R1921 100K PM_SLP_S4_L
R1922 100K PM_SLP_S5_L
R1923 100K PM_SLP_SUS_L
R1981 100K LVDS_IG_BKL_ON
R1984 100K LVDS_IG_PANEL_PWR
U1800
PANTHERPOINT
MOBILE
FCBGA
(4 OF 10)
LVDS
DIGITAL DISPLAY INTERFACE
CRT
OMIT_TABLE
LVDS_IG_BKL_ON
LVDS_IG_PANEL_PWR
LVDS_IG_BKL_PWM
LVDS_IG_DDC_CLK
LVDS_IG_DDC_DATA
TP_LVDS_IG_CTRL_CLK
TP_LVDS_IG_CTRL_DATA
PCH_LVDS_IBG
TP_PCH_LVDS_VBG
PLACE_NEAR=U1800.AF37:2.54mm
R1950 2.37K
LVDS_IG_A_CLK_N
LVDS_IG_A_CLK_P
LVDS_IG_A_DATA_N<0>
LVDS_IG_A_DATA_N<1>
LVDS_IG_A_DATA_N<2>
LVDS_IG_A_DATA_N<3>
LVDS_IG_A_DATA_P<0>
LVDS_IG_A_DATA_P<1>
LVDS_IG_A_DATA_P<2>
LVDS_IG_A_DATA_P<3>
LVDS_IG_B_CLK_N
LVDS_IG_B_CLK_P
LVDS_IG_B_DATA_N<0>
LVDS_IG_B_DATA_N<1>
LVDS_IG_B_DATA_N<2>
LVDS_IG_B_DATA_N<3>
LVDS_IG_B_DATA_P<0>
LVDS_IG_B_DATA_P<1>
LVDS_IG_B_DATA_P<2>
LVDS_IG_B_DATA_P<3>
TP_CRT_IG_BLUE
TP_CRT_IG_GREEN
TP_CRT_IG_RED
TP_CRT_IG_DDC_CLK
TP_CRT_IG_DDC_DATA
TP_CRT_IG_HSYNC
TP_CRT_IG_VSYNC
PCH_DAC_IREF
PLACE_NEAR=U1800.T43:2.54mm
R1951 1K
L_BKLTEN
L_VDD_EN
L_BKLTCTL
L_DDC_CLK
L_DDC_DATA (IPD-PLTRST#)
L_CTRL_CLK
L_CTRL_DATA
LVD_IBG
LVD_VBG
LVD_VREFH
LVD_VREFL
LVDSA_CLK*
LVDSA_CLK
LVDSA_DATA0*
LVDSA_DATA1*
LVDSA_DATA2*
LVDSA_DATA3*
LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3
LVDSB_CLK*
LVDSB_CLK
LVDSB_DATA0*
LVDSB_DATA1*
LVDSB_DATA2*
LVDSB_DATA3*
LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
LVDSB_DATA3
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_VSYNC
DAC_IREF
CRT_IRTN
SDVO_TVCLKINN (IPD)
SDVO_TVCLKINP (IPD)
SDVO_STALLN (IPD)
SDVO_STALLP (IPD)
SDVO_INTN (IPD)
SDVO_INTP (IPD)
SDVO_CTRLCLK
SDVO_CTRLDATA (IPD-PLTRST#)
DDPB_AUXN
DDPB_AUXP
DDPB_HPD
DDPB_0N
DDPB_0P
DDPB_1N
DDPB_1P
DDPB_2N
DDPB_2P
DDPB_3N
DDPB_3P
DDPC_CTRLCLK
DDPC_CTRLDATA (IPD-PLTRST#)
DDPC_AUXN
DDPC_AUXP
DDPC_HPD
DDPC_0N
DDPC_0P
DDPC_1N
DDPC_1P
DDPC_2N
DDPC_2P
DDPC_3N
DDPC_3P
DDPD_CTRLCLK
DDPD_CTRLDATA (IPD-PLTRST#)
DDPD_AUXN
DDPD_AUXP
DDPD_HPD
DDPD_0N
DDPD_0P
DDPD_1N
DDPD_1P
DDPD_2N
DDPD_2P
DDPD_3N
DDPD_3P
TP_SDVO_TVCLKINN
TP_SDVO_TVCLKINP
TP_SDVO_STALLN
TP_SDVO_STALLP
TP_SDVO_INTN
TP_SDVO_INTP
DPA_IG_DDC_CLK
DPA_IG_DDC_DATA
DPA_IG_AUX_CH_N
DPA_IG_AUX_CH_P
DPA_IG_HPD
TP_DP_IG_B_MLN<0>
TP_DP_IG_B_MLP<0>
TP_DP_IG_B_MLN<1>
TP_DP_IG_B_MLP<1>
TP_DP_IG_B_MLN<2>
TP_DP_IG_B_MLP<2>
TP_DP_IG_B_MLN<3>
TP_DP_IG_B_MLP<3>
DPB_IG_DDC_CLK
DPB_IG_DDC_DATA
DPB_IG_AUX_CH_N
DPB_IG_AUX_CH_P
DPB_IG_HPD
TP_DP_IG_C_MLN<0>
TP_DP_IG_C_MLP<0>
TP_DP_IG_C_MLN<1>
TP_DP_IG_C_MLP<1>
TP_DP_IG_C_MLN<2>
TP_DP_IG_C_MLP<2>
TP_DP_IG_C_MLN<3>
TP_DP_IG_C_MLP<3>
TP_DP_IG_D_CTRL_CLK
TP_DP_IG_D_CTRL_DATA
TP_DP_IG_D_AUXN
TP_DP_IG_D_AUXP
TP_DP_IG_D_HPD
TP_DP_IG_D_MLN<0>
TP_DP_IG_D_MLP<0>
TP_DP_IG_D_MLN<1>
TP_DP_IG_D_MLP<1>
TP_DP_IG_D_MLN<2>
TP_DP_IG_D_MLP<2>
TP_DP_IG_D_MLN<3>
TP_DP_IG_D_MLP<3>
SYNC_MASTER=J31_MLB
SYNC_DATE=06/13/2011
PAGE TITLE
PCH DMI/FDI/PM/Graphics
Apple Inc.
DRAWING NUMBER 051-9058
SIZE D
REVISION 6.0.0
BRANCH
PAGE 19 OF 109
SHEET 17 OF 86
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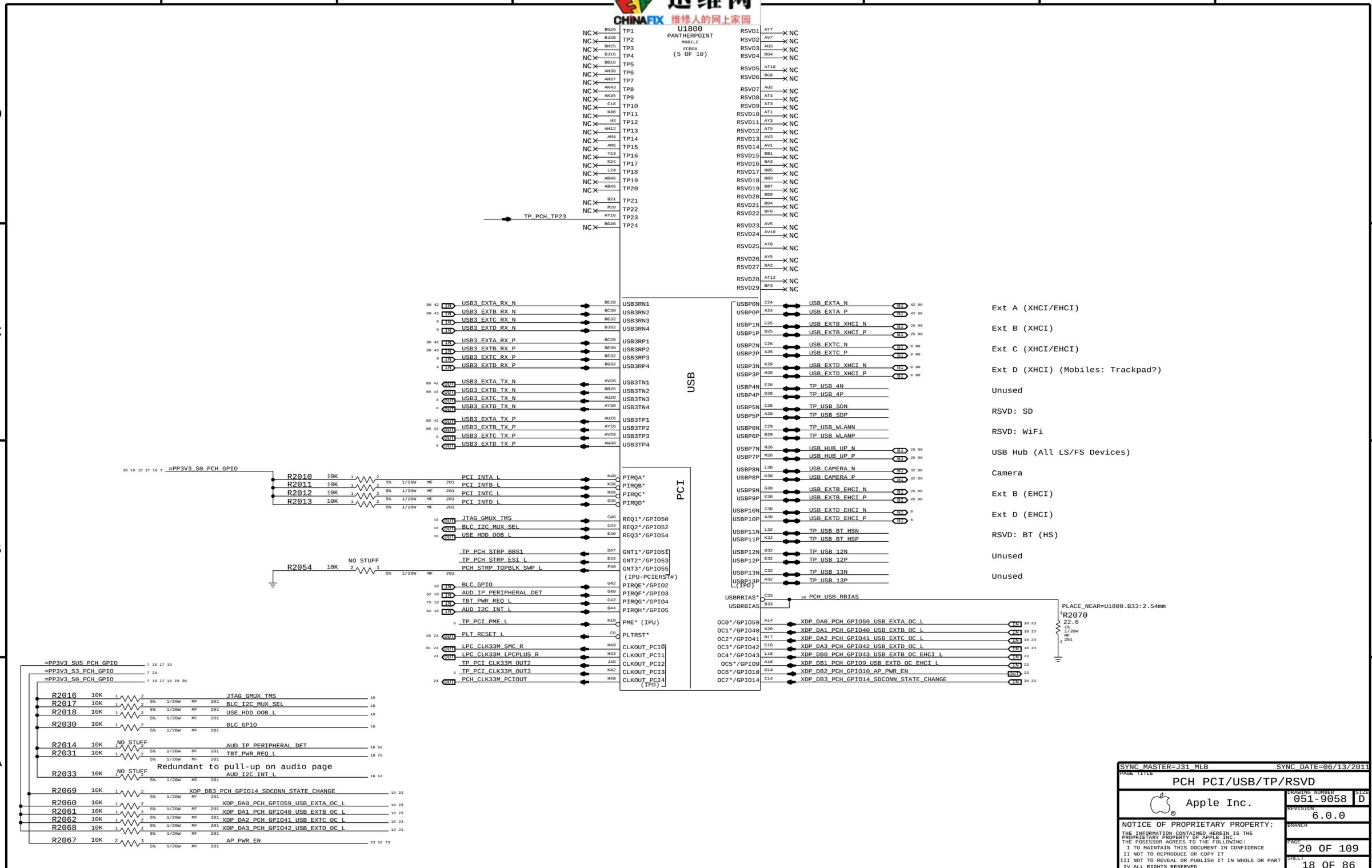

Ext A (XHCI/EHCI)

Ext B (XHCI)

Ext C (XHCI/EHCI)

Ext D (XHCI) (Mobiles: Trackpad?)

Unused

RSVD: SD

RSVD: WiFi

USB Hub (All LS/FS Devices)

Camera

Ext B (EHCI)

Ext D (EHCI)

RSVD: BT (HS)

Unused

Unused

SYNC MASTER=J31 MLB SYNC DATE=06/13/2011

PAGE TITLE
PCH PCI/USB/TP/RSVD

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

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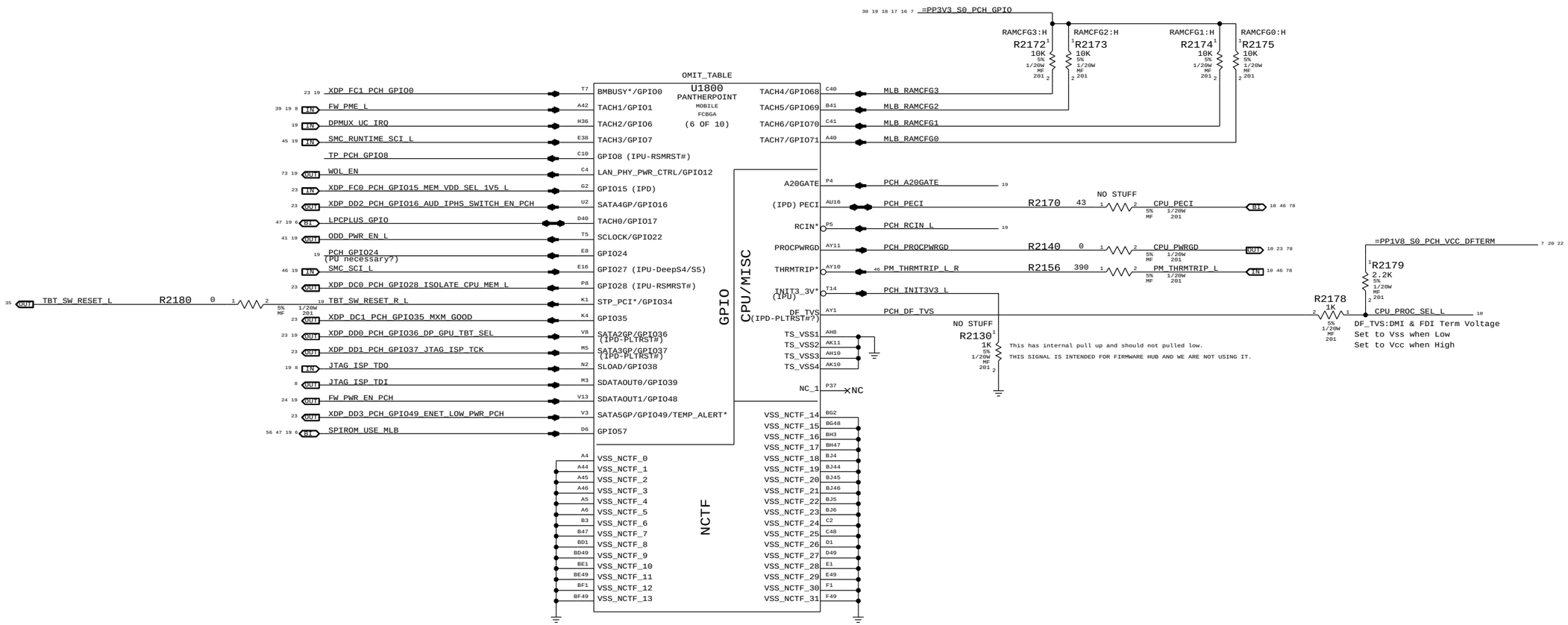
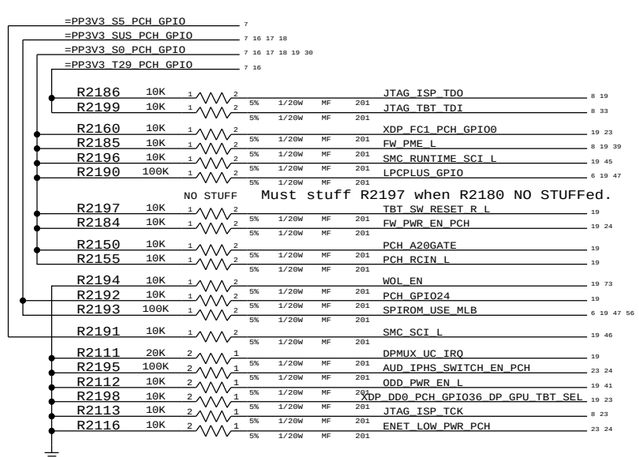
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.





SYNC_MASTER=J31_MLB SYNC_DATE=06/13/2011

PAGE TITLE: PCH GPIO/MISC/NCTF

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

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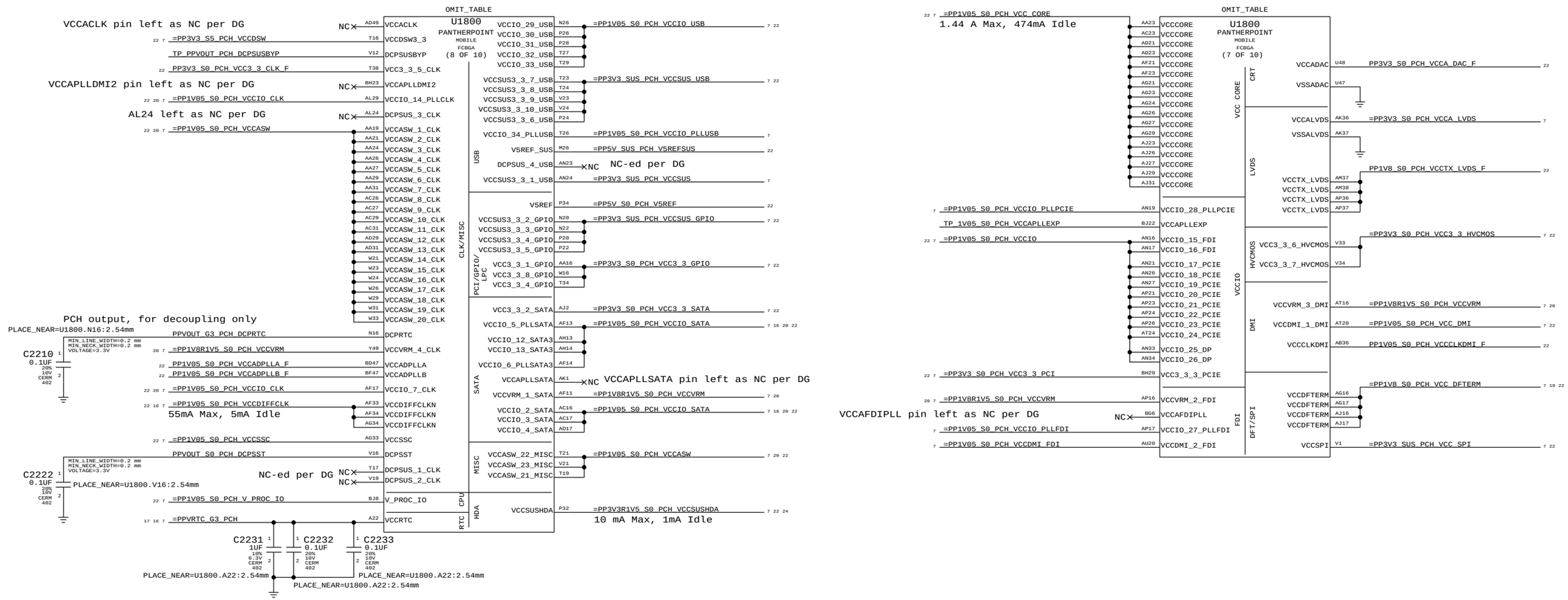

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PAGE TITLE	PCH POWER
Apple Inc.	DRAWING NUMBER 051-9058 SIZE D
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OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
FCBGA
(9 OF 10)
VSS

H5	VSS	VSS	AK38
AA17	VSS	VSS	AK4
AA2	VSS	VSS	AK42
AA3	VSS	VSS	AK46
AA33	VSS	VSS	AK8
AA34	VSS	VSS	AL16
AB11	VSS	VSS	AL17
AB14	VSS	VSS	AL19
AB39	VSS	VSS	AL2
AB4	VSS	VSS	AL21
AB43	VSS	VSS	AL23
AB5	VSS	VSS	AL26
AB7	VSS	VSS	AL27
AC19	VSS	VSS	AL31
AC2	VSS	VSS	AL33
AC21	VSS	VSS	AL34
AC24	VSS	VSS	AL48
AC33	VSS	VSS	AM11
AC34	VSS	VSS	AM14
AC48	VSS	VSS	AM36
AD10	VSS	VSS	AM39
AD11	VSS	VSS	AM43
AD12	VSS	VSS	AM45
AD13	VSS	VSS	AM46
AD19	VSS	VSS	AM7
AD24	VSS	VSS	AN2
AD26	VSS	VSS	AN29
AD27	VSS	VSS	AN3
AD33	VSS	VSS	AN31
AD34	VSS	VSS	AP12
AD36	VSS	VSS	AP19
AD37	VSS	VSS	AP28
AD38	VSS	VSS	AP30
AD39	VSS	VSS	AP32
AD4	VSS	VSS	AP38
AD40	VSS	VSS	AP4
AD42	VSS	VSS	AP42
AD43	VSS	VSS	AP46
AD45	VSS	VSS	AP8
AD46	VSS	VSS	AR2
AD8	VSS	VSS	AR48
AE2	VSS	VSS	AT11
AE3	VSS	VSS	AT13
AF10	VSS	VSS	AT18
AF12	VSS	VSS	AT22
AD14	VSS	VSS	AT26
AD16	VSS	VSS	AT28
AF16	VSS	VSS	AT30
AF19	VSS	VSS	AT32
AF24	VSS	VSS	AT34
AF26	VSS	VSS	AT39
AF27	VSS	VSS	AT42
AF29	VSS	VSS	AT46
AF31	VSS	VSS	AT7
AF38	VSS	VSS	AU24
AF4	VSS	VSS	AU30
AF42	VSS	VSS	AV11
AF46	VSS	VSS	AV16
AF5	VSS	VSS	AV20
AF7	VSS	VSS	AV24
AF8	VSS	VSS	AV30
AG19	VSS	VSS	AV38
AG2	VSS	VSS	AV4
AG31	VSS	VSS	AV43
AG48	VSS	VSS	AV8
AH11	VSS	VSS	AW14
AH3	VSS	VSS	AW18
AH36	VSS	VSS	AW2
AH39	VSS	VSS	AW22
AH40	VSS	VSS	AW26
AH42	VSS	VSS	AW28
AH46	VSS	VSS	AW32
AH7	VSS	VSS	AW34
AJ19	VSS	VSS	AW36
AJ21	VSS	VSS	AW40
AJ24	VSS	VSS	AW48
AJ33	VSS	VSS	AY12
AJ34	VSS	VSS	AY22
AK12	VSS	VSS	AY28
AK3	VSS		

OMIT_TABLE

U1800
PANTHERPOINT
MOBILE
FCBGA
(10 OF 10)
VSS

AY4	VSS	VSS	H46
AY42	VSS	VSS	K18
AY46	VSS	VSS	K26
AY8	VSS	VSS	K39
B11	VSS	VSS	K46
B15	VSS	VSS	K7
B19	VSS	VSS	L18
B23	VSS	VSS	L2
B27	VSS	VSS	L20
B31	VSS	VSS	L26
B35	VSS	VSS	L28
B39	VSS	VSS	L36
B7	VSS	VSS	L48
F45	VSS	VSS	M12
BB12	VSS	VSS	P16
BB16	VSS	VSS	M18
BB20	VSS	VSS	M22
BB22	VSS	VSS	M24
BB24	VSS	VSS	M30
BB28	VSS	VSS	M32
BB30	VSS	VSS	M34
BB38	VSS	VSS	M38
BB4	VSS	VSS	M4
BB46	VSS	VSS	M42
BC14	VSS	VSS	M46
BC18	VSS	VSS	M8
BC2	VSS	VSS	N18
BC22	VSS	VSS	P30
BC26	VSS	VSS	N47
BC32	VSS	VSS	P11
BC34	VSS	VSS	P18
BC36	VSS	VSS	T33
BC40	VSS	VSS	P40
BC42	VSS	VSS	P43
BC48	VSS	VSS	P47
BD46	VSS	VSS	P7
BD5	VSS	VSS	R2
BE22	VSS	VSS	R48
BE26	VSS	VSS	T12
BE40	VSS	VSS	T31
BF10	VSS	VSS	T37
BF12	VSS	VSS	T4
BF16	VSS	VSS	W34
BF20	VSS	VSS	T46
BF22	VSS	VSS	T47
BF24	VSS	VSS	T8
BF26	VSS	VSS	V11
BF28	VSS	VSS	V17
BD3	VSS	VSS	V26
BF30	VSS	VSS	V27
BF38	VSS	VSS	V29
BF40	VSS	VSS	V31
BF8	VSS	VSS	V36
BG17	VSS	VSS	V39
BG21	VSS	VSS	V43
BG33	VSS	VSS	V7
BG44	VSS	VSS	W17
BG8	VSS	VSS	W19
BH11	VSS	VSS	W2
BH15	VSS	VSS	W27
BH17	VSS	VSS	W48
BH19	VSS	VSS	Y12
H10	VSS	VSS	Y38
BH27	VSS	VSS	Y4
BH31	VSS	VSS	Y42
BH33	VSS	VSS	Y46
BH35	VSS	VSS	Y8
BH39	VSS		
BH43	VSS		
BH7	VSS	VSS	BG29
D3	VSS	VSS	N24
D12	VSS	VSS	AJ3
D16	VSS	VSS	AD47
D18	VSS		
D22	VSS	VSS	B43
D24	VSS	VSS	BE10
D26	VSS	VSS	BG41
D30	VSS		
D32	VSS	VSS	G14
D34	VSS	VSS	H16
D38	VSS		
D42	VSS	VSS	T36
D8	VSS		
E18	VSS	VSS	BG22
E26	VSS	VSS	BG24
G18	VSS	VSS	C22
G20	VSS	VSS	AP13
G26	VSS	VSS	M14
G28	VSS	VSS	AP3
G36	VSS	VSS	AP1
G48	VSS	VSS	BE16
H12	VSS	VSS	BC16
H18	VSS	VSS	BG28
H22	VSS	VSS	BJ28
H24	VSS		
H26	VSS		
H30	VSS		
H32	VSS		
H34	VSS		
F3	VSS		

SYNC_MASTER=J31_MLB SYNC_DATE=06/13/2011

PAGE TITLE
PCH GROUNDS

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DRAWING NUMBER 051-9058 SIZE D

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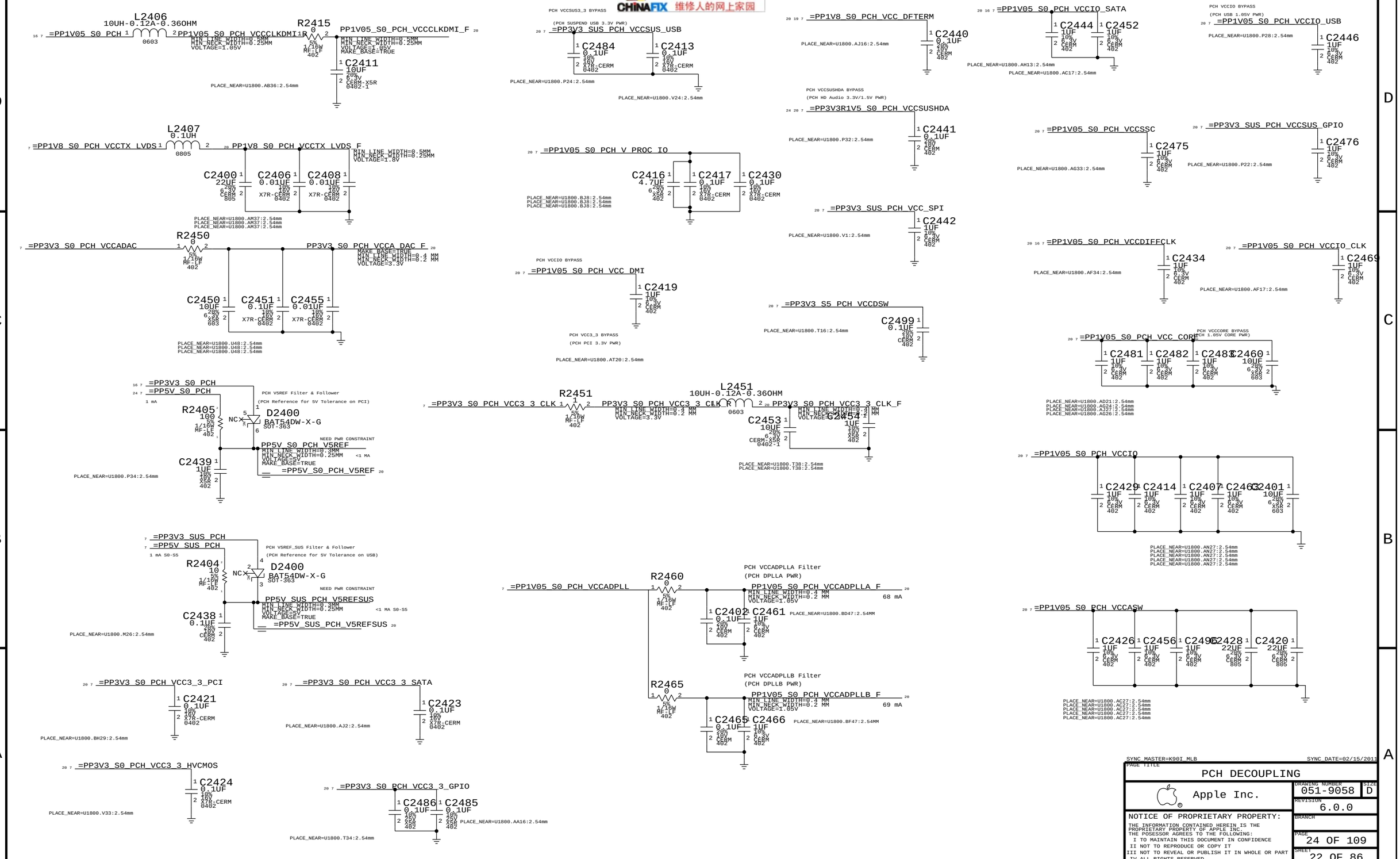

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2013

PAGE TITLE: PCH DECOUPLING

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DRAWING NUMBER: 051-9058 SIZE: D

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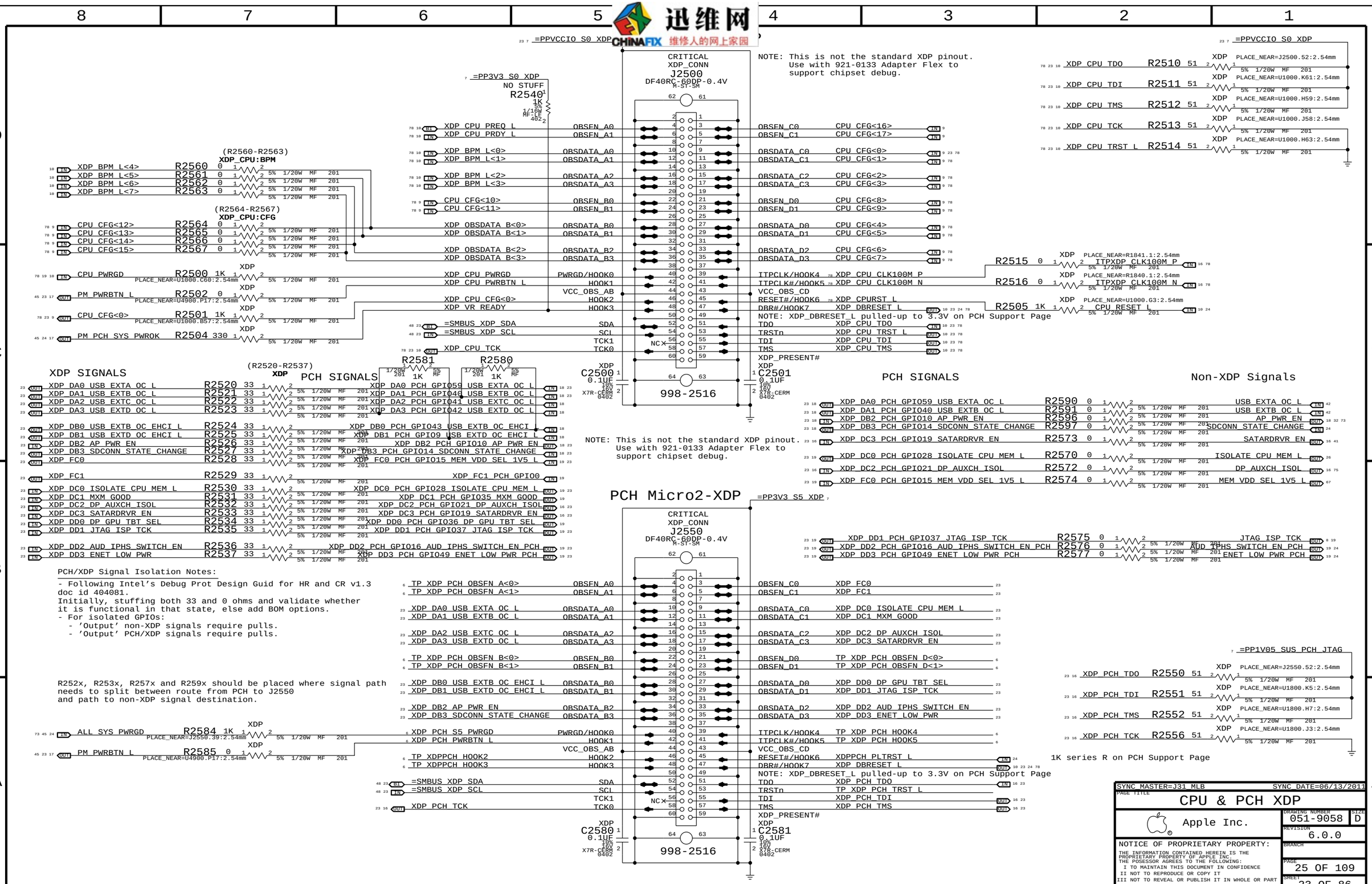
CRITICAL
XDP_CONN
J2500
DF40RC-60DP-0.4V
M-ST-SM
998-2516
NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.
=PPVCCIO_S0_XDP
=PP3V3_S0_XDP
NO STUFF
R2540 1K 5% 1/16W MF-LF 402
(R2560-R2563)
XDP_CPU:BPM
XDP_BPM_L<4> R2560 0
XDP_BPM_L<5> R2561 0
XDP_BPM_L<6> R2562 0
XDP_BPM_L<7> R2563 0
(R2564-R2567)
XDP_CPU:CFG
CPU_CFG<12> R2564 0
CPU_CFG<13> R2565 0
CPU_CFG<14> R2566 0
CPU_CFG<15> R2567 0
CPU_PWRGD R2500 1K
PLACE_NEAR=U1000.C60:2.54mm
PM_PWRBTN_L R2502 0
PLACE_NEAR=U4900.P17:2.54mm
CPU_CFG<0> R2501 1K
PLACE_NEAR=U1000.B57:2.54mm
PM_PCH_SYS_PWROK R2504 330
XDP_CPU_PREQ_L
XDP_CPU_PRDY_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
CPU_CFG<10>
CPU_CFG<11>
XDP_OBSDATA_B<0>
XDP_OBSDATA_B<1>
XDP_OBSDATA_B<2>
XDP_OBSDATA_B<3>
XDP_CPU_PWRGD
XDP_CPU_PWRBTN_L
XDP_CPU_CFG<0>
XDP_VR_READY
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_CPU_TCK
OBSFN_A0
OBSFN_A1
OBSDATA_A0
OBSDATA_A1
OBSDATA_A2
OBSDATA_A3
OBSFN_B0
OBSFN_B1
OBSDATA_B0
OBSDATA_B1
OBSDATA_B2
OBSDATA_B3
PWRGD/HOOK0
HOOK1
VCC_OBS_AB
HOOK2
HOOK3
SDA
SCL
TCK1
TCK0
NC
OBSFN_C0
OBSFN_C1
OBSDATA_C0
OBSDATA_C1
OBSDATA_C2
OBSDATA_C3
OBSFN_D0
OBSFN_D1
OBSDATA_D0
OBSDATA_D1
OBSDATA_D2
OBSDATA_D3
ITPCLK/HOOK4
ITPCLK#/HOOK5
VCC_OBS_CD
RESET#/HOOK6
DBR#/HOOK7
TDO
TRSTn
TDI
TMS
XDP_PRESENT#
CPU_CFG<16>
CPU_CFG<17>
CPU_CFG<0>
CPU_CFG<1>
CPU_CFG<2>
CPU_CFG<3>
CPU_CFG<8>
CPU_CFG<9>
CPU_CFG<4>
CPU_CFG<5>
CPU_CFG<6>
CPU_CFG<7>
XDP_CPU_CLK100M_P
XDP_CPU_CLK100M_N
XDP_CPURST_L
XDP_DBRESET_L
NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page
XDP_CPU_TDO
XDP_CPU_TRST_L
XDP_CPU_TDI
XDP_CPU_TMS
C2500 0.1UF 10V X7R-CERM 0402
C2501 0.1UF 10V X7R-CERM 0402
XDP_CPU_TDO R2510 51
XDP_CPU_TDI R2511 51
XDP_CPU_TMS R2512 51
XDP_CPU_TCK R2513 51
XDP_CPU_TRST_L R2514 51
PLACE_NEAR=J2500.52:2.54mm
PLACE_NEAR=U1000.K61:2.54mm
PLACE_NEAR=U1000.H59:2.54mm
PLACE_NEAR=U1000.J58:2.54mm
PLACE_NEAR=U1000.H63:2.54mm
R2515 0 ITPXDP_CLK100M_P
R2516 0 ITPXDP_CLK100M_N
R2505 1K CPU_RESET_L
PLACE_NEAR=R1841.1:2.54mm
PLACE_NEAR=R1840.1:2.54mm
PLACE_NEAR=U1000.G3:2.54mm
XDP SIGNALS
(R2520-R2537)
XDP_DA0_USB_EXTA_OC_L R2520 33
XDP_DA1_USB_EXTB_OC_L R2521 33
XDP_DA2_USB_EXTC_OC_L R2522 33
XDP_DA3_USB_EXTD_OC_L R2523 33
XDP_DB0_USB_EXTB_OC_EHCI_L R2524 33
XDP_DB1_USB_EXTD_OC_EHCI_L R2525 33
XDP_DB2_AP_PWR_EN R2526 33
XDP_DB3_SDCONN_STATE_CHANGE R2527 33
XDP_FC0 R2528 33
XDP_FC1 R2529 33
XDP_DC0_ISOLATE_CPU_MEM_L R2530 33
XDP_DC1_MXM_GOOD R2531 33
XDP_DC2_DP_AUXCH_ISOL R2532 33
XDP_DC3_SATARDRVR_EN R2533 33
XDP_DD0_DP_GPU_TBT_SEL R2534 33
XDP_DD1_JTAG_ISP_TCK R2535 33
XDP_DD2_AUD_IPHS_SWITCH_EN R2536 33
XDP_DD3_ENET_LOW_PWR R2537 33
PCH SIGNALS
R2581 1K
R2580 1K
XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L
XDP_DA2_PCH_GPIO41_USB_EXTC_OC_L
XDP_DA3_PCH_GPIO42_USB_EXTD_OC_L
XDP_DB0_PCH_GPIO43_USB_EXTB_OC_EHCI
XDP_DB1_PCH_GPIO9_USB_EXTD_OC_EHCI_L
XDP_DB2_PCH_GPIO10_AP_PWR_EN
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE
XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L
XDP_FC1_PCH_GPIO0
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L
XDP_DC1_PCH_GPIO35_MXM_GOOD
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL
XDP_DC3_PCH_GPIO19_SATARDRVR_EN
XDP_DD0_PCH_GPIO36_DP_GPU_TBT_SEL
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH
PCH SIGNALS
XDP_DA0_PCH_GPIO59_USB_EXTA_OC_L R2590 0
XDP_DA1_PCH_GPIO40_USB_EXTB_OC_L R2591 0
XDP_DB2_PCH_GPIO10_AP_PWR_EN R2596 0
XDP_DB3_PCH_GPIO14_SDCONN_STATE_CHANGE R2597 0
XDP_DC3_PCH_GPIO19_SATARDRVR_EN R2573 0
XDP_DC0_PCH_GPIO28_ISOLATE_CPU_MEM_L R2570 0
XDP_DC2_PCH_GPIO21_DP_AUXCH_ISOL R2572 0
XDP_FC0_PCH_GPIO15_MEM_VDD_SEL_1V5_L R2574 0
Non-XDP Signals
USB_EXTA_OC_L
USB_EXTB_OC_L
AP_PWR_EN
SDCONN_STATE_CHANGE
SATARDRVR_EN
ISOLATE_CPU_MEM_L
DP_AUXCH_ISOL
MEM_VDD_SEL_1V5_L
XDP_DD1_PCH_GPIO37_JTAG_ISP_TCK R2575 0
XDP_DD2_PCH_GPIO16_AUD_IPHS_SWITCH_EN_PCH R2576 0
XDP_DD3_PCH_GPIO49_ENET_LOW_PWR_PCH R2577 0
JTAG_ISP_TCK
AUD_IPHS_SWITCH_EN_PCH
ENET_LOW_PWR_PCH
PCH Micro2-XDP
=PP3V3_S5_XDP
PCH/XDP Signal Isolation Notes:
- Following Intel's Debug Prot Design Guid for HR and CR v1.3
doc id 404081.
Initially, stuffing both 33 and 0 ohms and validate whether
it is functional in that state, else add BOM options.
- For isolated GPIOs:
- 'Output' non-XDP signals require pulls.
- 'Output' PCH/XDP signals require pulls.
R252x, R253x, R257x and R259x should be placed where signal path
needs to split between route from PCH to J2550
and path to non-XDP signal destination.
ALL_SYS_PWRGD R2584 1K
PM_PWRBTN_L R2585 0
PLACE_NEAR=J2550.39:2.54mm
PLACE_NEAR=U4900.P17:2.54mm
TP_XDP_PCH_OBSFN_A<0>
TP_XDP_PCH_OBSFN_A<1>
XDP_DA0_USB_EXTA_OC_L
XDP_DA1_USB_EXTB_OC_L
XDP_DA2_USB_EXTC_OC_L
XDP_DA3_USB_EXTD_OC_L
TP_XDP_PCH_OBSFN_B<0>
TP_XDP_PCH_OBSFN_B<1>
XDP_DB0_USB_EXTB_OC_EHCI_L
XDP_DB1_USB_EXTD_OC_EHCI_L
XDP_DB2_AP_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE
XDP_PCH_S5_PWRGD
XDP_PCH_PWRBTN_L
TP_XDPPCH_HOOK2
TP_XDPPCH_HOOK3
=SMBUS_XDP_SDA
=SMBUS_XDP_SCL
XDP_PCH_TCK
XDP_FC0
XDP_FC1
XDP_DC0_ISOLATE_CPU_MEM_L
XDP_DC1_MXM_GOOD
XDP_DC2_DP_AUXCH_ISOL
XDP_DC3_SATARDRVR_EN
XDP_DD0_DP_GPU_TBT_SEL
XDP_DD1_JTAG_ISP_TCK
XDP_DD2_AUD_IPHS_SWITCH_EN
XDP_DD3_ENET_LOW_PWR
XDPPCH_PLTRST_L
XDP_PCH_TDO
TP_XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS
C2580 0.1UF 10V X7R-CERM 0402
C2581 0.1UF 10V X7R-CERM 0402
=PP1V05_SUS_PCH_JTAG
XDP_PCH_TDO R2550 51
XDP_PCH_TDI R2551 51
XDP_PCH_TMS R2552 51
XDP_PCH_TCK R2556 51
PLACE_NEAR=J2550.52:2.54mm
PLACE_NEAR=U1800.K5:2.54mm
PLACE_NEAR=U1800.H7:2.54mm
PLACE_NEAR=U1800.J3:2.54mm
1K series R on PCH Support Page
SYNC_MASTER=J31_MLB
SYNC_DATE=06/13/2011
PAGE TITLE
CPU & PCH XDP
Apple Inc.
DRAWING NUMBER 051-9058
SIZE D
REVISION 6.0.0
BRANCH
PAGE 25 OF 109
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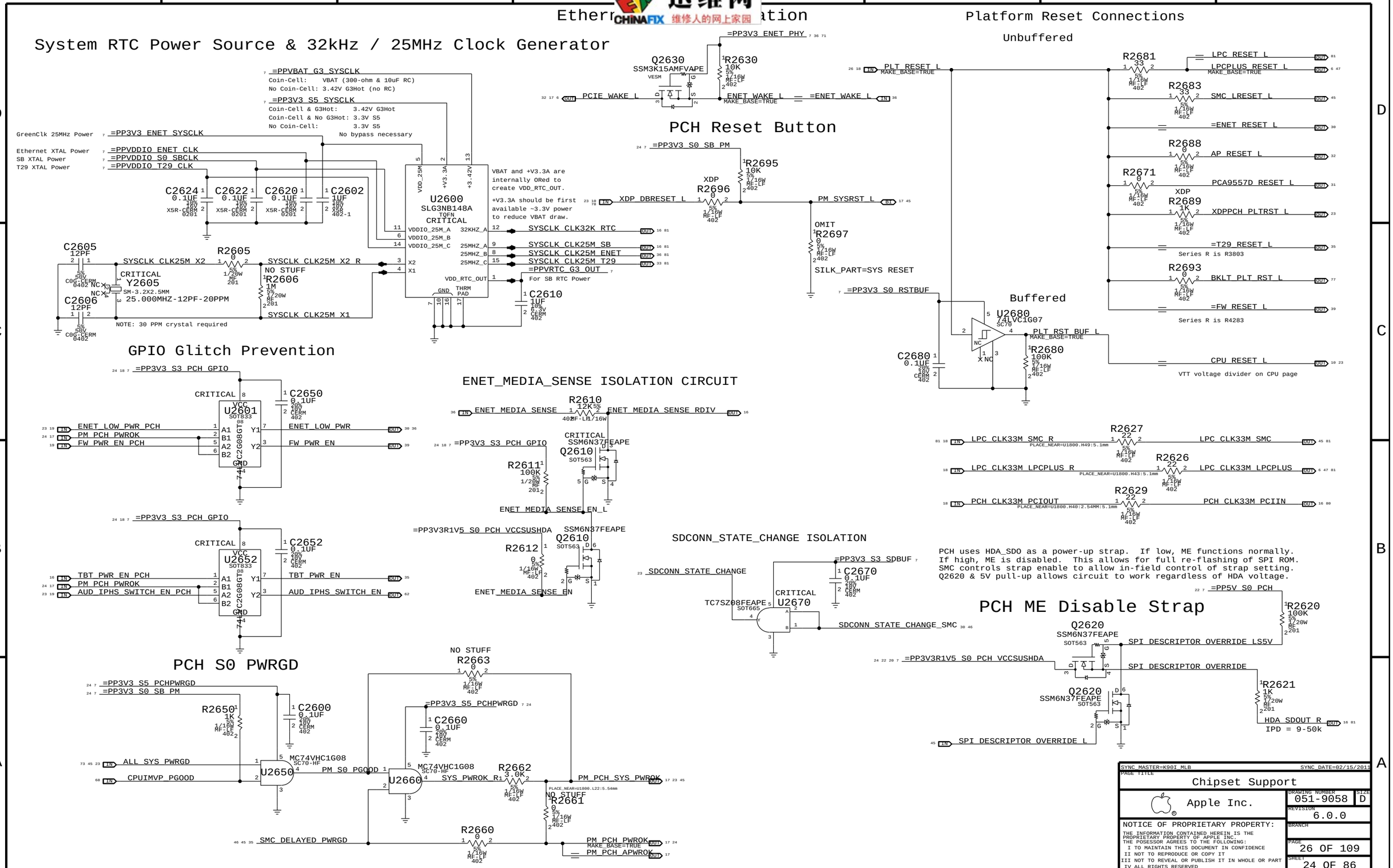

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE: Chipset Support

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DRAWING NUMBER: 051-9058 SIZE: D

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BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

USB MUX FOR LS/FS INTERNAL DEVICES

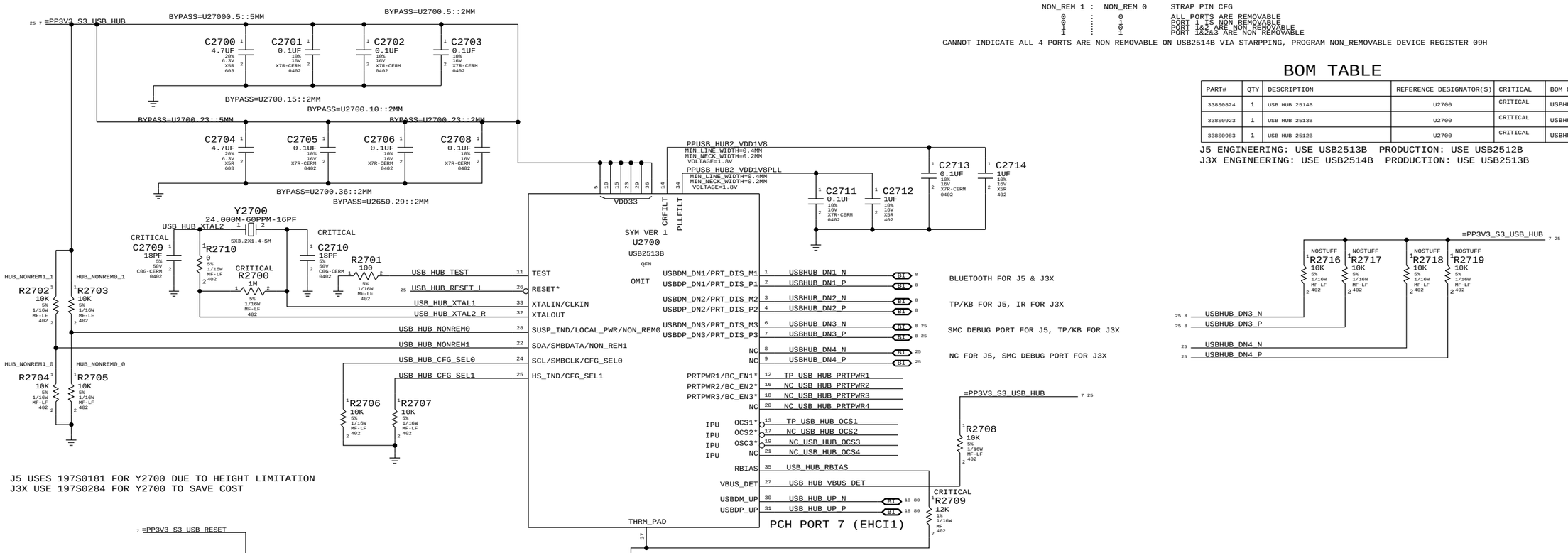
NON_REM 1 : NON_REM 0 STRAP PIN CFG
0 : 0 ALL PORTS ARE REMOVABLE
0 : 1 PORT 1 IS NON REMOVABLE
1 : 0 PORT 1&2 ARE NON REMOVABLE
1 : 1 PORT 1&2&3 ARE NON REMOVABLE

CANNOT INDICATE ALL 4 PORTS ARE NON REMOVABLE ON USB2514B VIA STARPPING, PROGRAM NON_REMOVABLE DEVICE REGISTER 09H

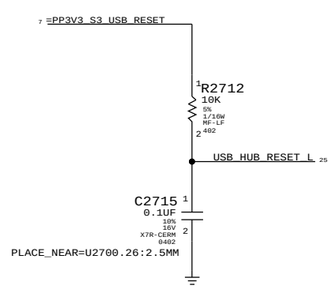
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33850824	1	USB HUB 2514B	U2700	CRITICAL	USBHUB2514B
33850923	1	USB HUB 2513B	U2700	CRITICAL	USBHUB2513B
33850983	1	USB HUB 2512B	U2700	CRITICAL	USBHUB2512B

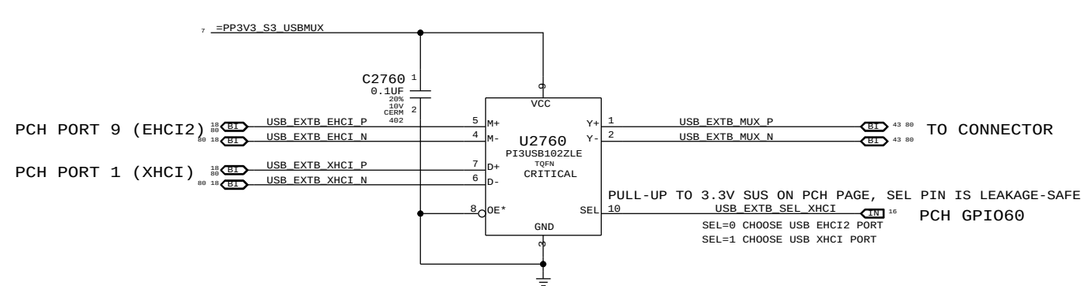
J5 ENGINEERING: USE USB2513B PRODUCTION: USE USB2512B
J3X ENGINEERING: USE USB2514B PRODUCTION: USE USB2513B



J5 USES 197S0181 FOR Y2700 DUE TO HEIGHT LIMITATION
J3X USE 197S0284 FOR Y2700 TO SAVE COST



USB XHCI/EHCI2 PORT MUX FOR EXT B



SYNC_MASTER=LINDA_J30 SYNC_DATE=09/19/2011

PAGE TITLE
USB HUB & MUX

Apple Inc.

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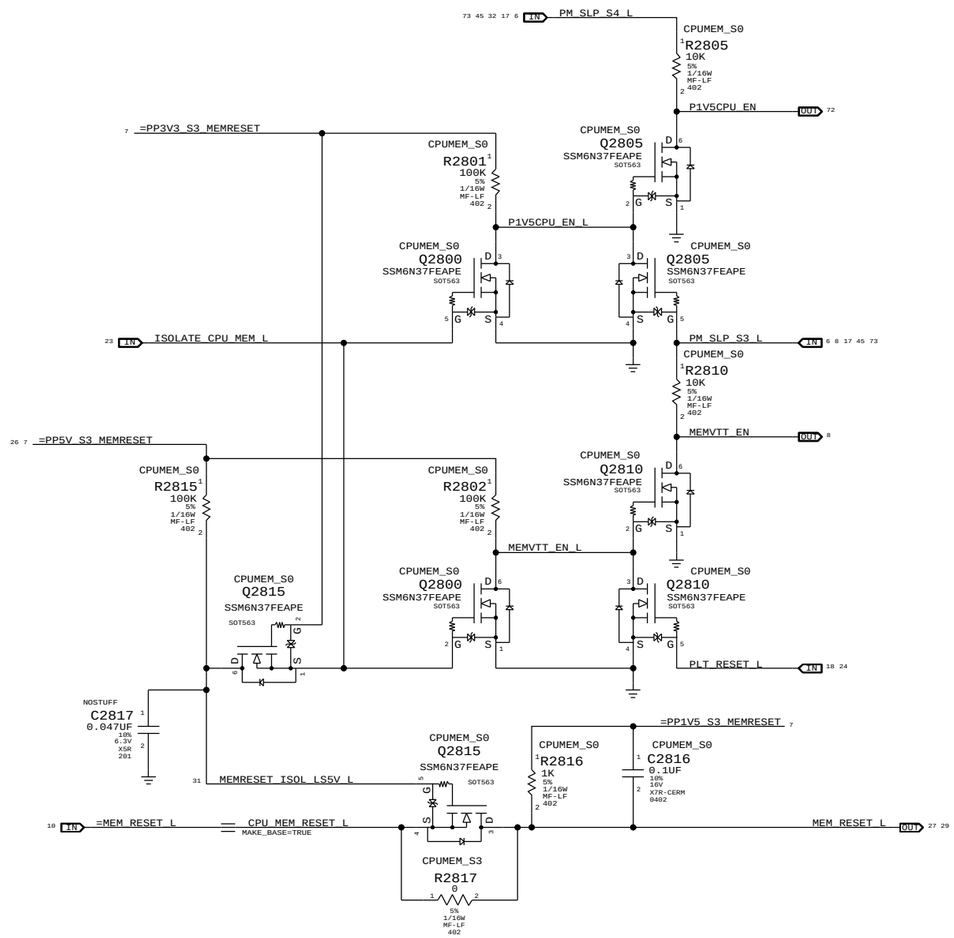
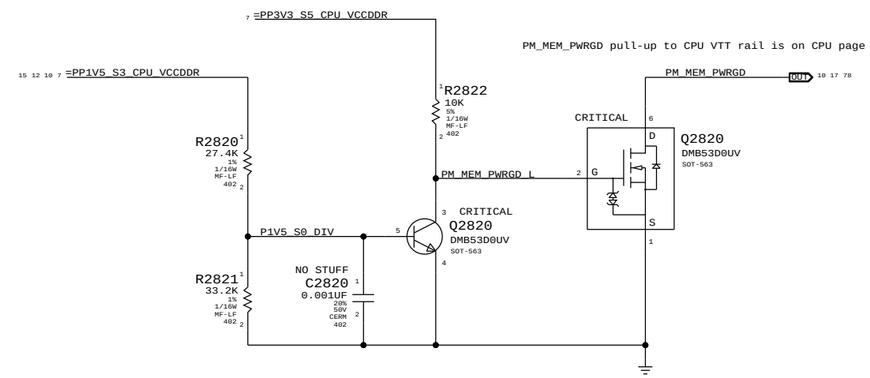
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

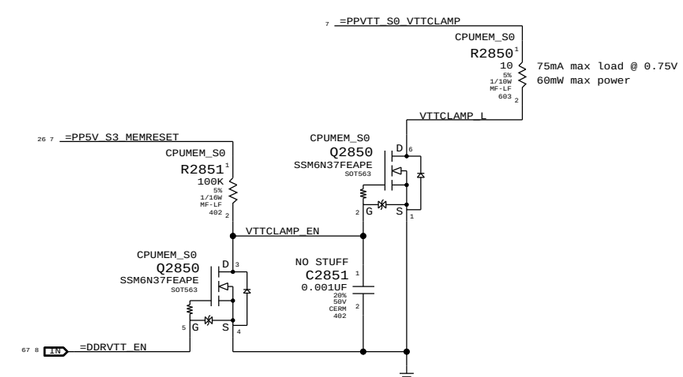


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	SOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
S3	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2013

PAGE TITLE
CPU Memory S3 Support

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D
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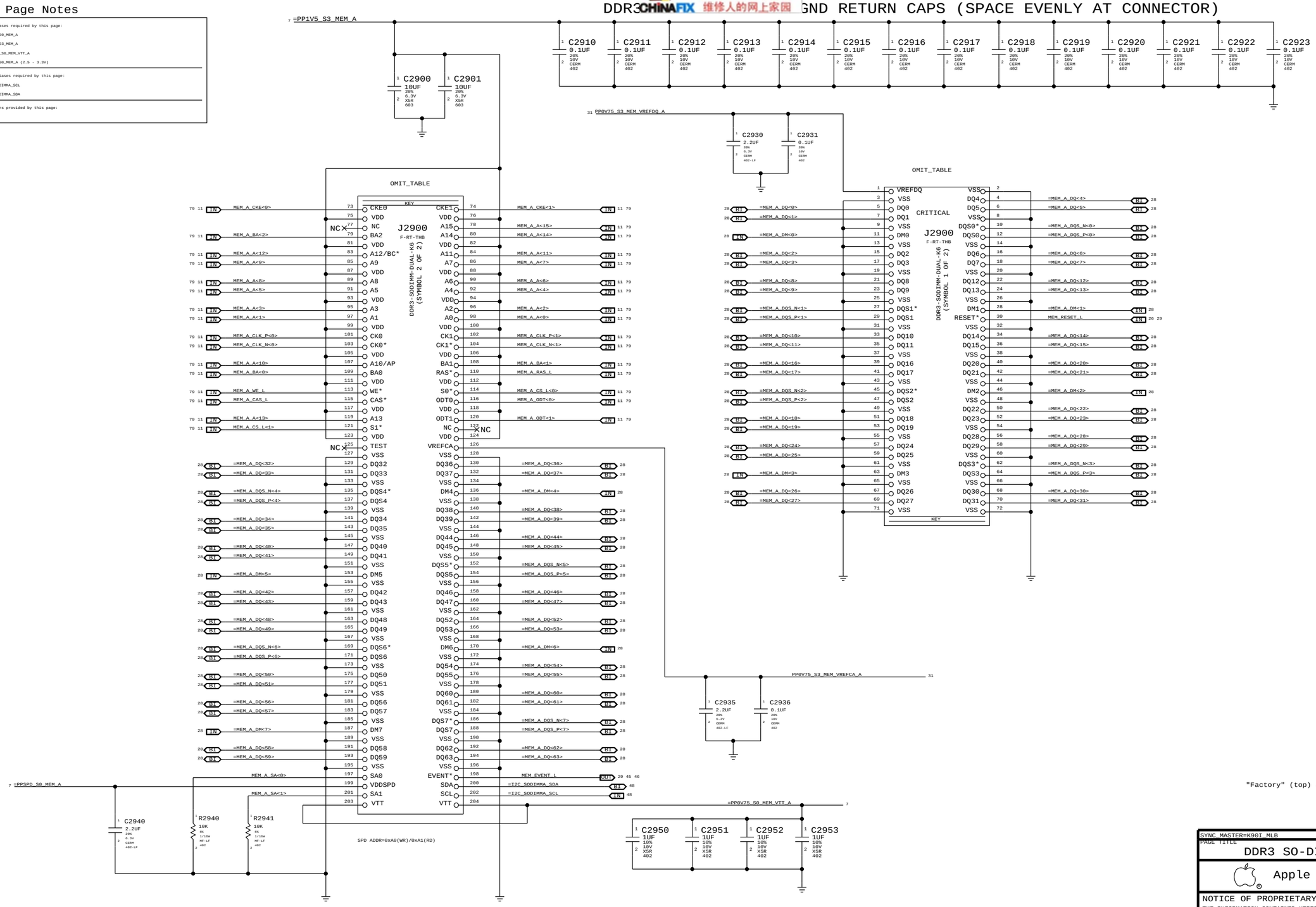
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PPSPD_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)



SYNC_MASTER=K90I_MLB	SYNC_DATE=02/15/2011
PAGE TITLE: DDR3 SO-DIMM Connector A	
Apple Inc.	DRAWING NUMBER: 051-9058 SIZE: D
	REVISION: 6.0.0
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CPU CHANNEL A DQS 0 -> DIMM A DQS 0

79 11	MEM_A_DQS_N<0>	MAKE_BASE=TRUE	=MEM_A_DQS_N<0>	27
79 11	MEM_A_DQS_P<0>	MAKE_BASE=TRUE	=MEM_A_DQS_P<0>	27
		MAKE_BASE=TRUE	=MEM_A_DM<0>	27
79 11	MEM_A_DQ<7>	MAKE_BASE=TRUE	=MEM_A_DQ<3>	27
79 11	MEM_A_DQ<6>	MAKE_BASE=TRUE	=MEM_A_DQ<6>	27
79 11	MEM_A_DQ<5>	MAKE_BASE=TRUE	=MEM_A_DQ<1>	27
79 11	MEM_A_DQ<4>	MAKE_BASE=TRUE	=MEM_A_DQ<5>	27
79 11	MEM_A_DQ<3>	MAKE_BASE=TRUE	=MEM_A_DQ<2>	27
79 11	MEM_A_DQ<2>	MAKE_BASE=TRUE	=MEM_A_DQ<7>	27
79 11	MEM_A_DQ<1>	MAKE_BASE=TRUE	=MEM_A_DQ<0>	27
79 11	MEM_A_DQ<0>	MAKE_BASE=TRUE	=MEM_A_DQ<4>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 1 -> DIMM A DQS 1

79 11	MEM_A_DQS_N<1>	MAKE_BASE=TRUE	=MEM_A_DQS_N<1>	27
79 11	MEM_A_DQS_P<1>	MAKE_BASE=TRUE	=MEM_A_DQS_P<1>	27
		MAKE_BASE=TRUE	=MEM_A_DM<1>	27
79 11	MEM_A_DQ<15>	MAKE_BASE=TRUE	=MEM_A_DQ<11>	27
79 11	MEM_A_DQ<14>	MAKE_BASE=TRUE	=MEM_A_DQ<10>	27
79 11	MEM_A_DQ<13>	MAKE_BASE=TRUE	=MEM_A_DQ<12>	27
79 11	MEM_A_DQ<12>	MAKE_BASE=TRUE	=MEM_A_DQ<9>	27
79 11	MEM_A_DQ<11>	MAKE_BASE=TRUE	=MEM_A_DQ<15>	27
79 11	MEM_A_DQ<10>	MAKE_BASE=TRUE	=MEM_A_DQ<14>	27
79 11	MEM_A_DQ<9>	MAKE_BASE=TRUE	=MEM_A_DQ<13>	27
79 11	MEM_A_DQ<8>	MAKE_BASE=TRUE	=MEM_A_DQ<8>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 2 -> DIMM A DQS 2

79 11	MEM_A_DQS_N<2>	MAKE_BASE=TRUE	=MEM_A_DQS_N<2>	27
79 11	MEM_A_DQS_P<2>	MAKE_BASE=TRUE	=MEM_A_DQS_P<2>	27
		MAKE_BASE=TRUE	=MEM_A_DM<2>	27
79 11	MEM_A_DQ<23>	MAKE_BASE=TRUE	=MEM_A_DQ<23>	27
79 11	MEM_A_DQ<22>	MAKE_BASE=TRUE	=MEM_A_DQ<22>	27
79 11	MEM_A_DQ<21>	MAKE_BASE=TRUE	=MEM_A_DQ<21>	27
79 11	MEM_A_DQ<20>	MAKE_BASE=TRUE	=MEM_A_DQ<20>	27
79 11	MEM_A_DQ<19>	MAKE_BASE=TRUE	=MEM_A_DQ<18>	27
79 11	MEM_A_DQ<18>	MAKE_BASE=TRUE	=MEM_A_DQ<19>	27
79 11	MEM_A_DQ<17>	MAKE_BASE=TRUE	=MEM_A_DQ<16>	27
79 11	MEM_A_DQ<16>	MAKE_BASE=TRUE	=MEM_A_DQ<17>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 3 -> DIMM A DQS 3

79 11	MEM_A_DQS_N<3>	MAKE_BASE=TRUE	=MEM_A_DQS_N<3>	27
79 11	MEM_A_DQS_P<3>	MAKE_BASE=TRUE	=MEM_A_DQS_P<3>	27
		MAKE_BASE=TRUE	=MEM_A_DM<3>	27
79 11	MEM_A_DQ<31>	MAKE_BASE=TRUE	=MEM_A_DQ<26>	27
79 11	MEM_A_DQ<30>	MAKE_BASE=TRUE	=MEM_A_DQ<24>	27
79 11	MEM_A_DQ<29>	MAKE_BASE=TRUE	=MEM_A_DQ<28>	27
79 11	MEM_A_DQ<28>	MAKE_BASE=TRUE	=MEM_A_DQ<25>	27
79 11	MEM_A_DQ<27>	MAKE_BASE=TRUE	=MEM_A_DQ<31>	27
79 11	MEM_A_DQ<26>	MAKE_BASE=TRUE	=MEM_A_DQ<27>	27
79 11	MEM_A_DQ<25>	MAKE_BASE=TRUE	=MEM_A_DQ<30>	27
79 11	MEM_A_DQ<24>	MAKE_BASE=TRUE	=MEM_A_DQ<29>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 4 -> DIMM A DQS 4

79 11	MEM_A_DQS_N<4>	MAKE_BASE=TRUE	=MEM_A_DQS_N<4>	27
79 11	MEM_A_DQS_P<4>	MAKE_BASE=TRUE	=MEM_A_DQS_P<4>	27
		MAKE_BASE=TRUE	=MEM_A_DM<4>	27
79 11	MEM_A_DQ<39>	MAKE_BASE=TRUE	=MEM_A_DQ<38>	27
79 11	MEM_A_DQ<38>	MAKE_BASE=TRUE	=MEM_A_DQ<39>	27
79 11	MEM_A_DQ<37>	MAKE_BASE=TRUE	=MEM_A_DQ<37>	27
79 11	MEM_A_DQ<36>	MAKE_BASE=TRUE	=MEM_A_DQ<33>	27
79 11	MEM_A_DQ<35>	MAKE_BASE=TRUE	=MEM_A_DQ<34>	27
79 11	MEM_A_DQ<34>	MAKE_BASE=TRUE	=MEM_A_DQ<35>	27
79 11	MEM_A_DQ<33>	MAKE_BASE=TRUE	=MEM_A_DQ<32>	27
79 11	MEM_A_DQ<32>	MAKE_BASE=TRUE	=MEM_A_DQ<36>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 5 -> DIMM A DQS 5

79 11	MEM_A_DQS_N<5>	MAKE_BASE=TRUE	=MEM_A_DQS_N<5>	27
79 11	MEM_A_DQS_P<5>	MAKE_BASE=TRUE	=MEM_A_DQS_P<5>	27
		MAKE_BASE=TRUE	=MEM_A_DM<5>	27
79 11	MEM_A_DQ<47>	MAKE_BASE=TRUE	=MEM_A_DQ<46>	27
79 11	MEM_A_DQ<46>	MAKE_BASE=TRUE	=MEM_A_DQ<43>	27
79 11	MEM_A_DQ<45>	MAKE_BASE=TRUE	=MEM_A_DQ<45>	27
79 11	MEM_A_DQ<44>	MAKE_BASE=TRUE	=MEM_A_DQ<41>	27
79 11	MEM_A_DQ<43>	MAKE_BASE=TRUE	=MEM_A_DQ<47>	27
79 11	MEM_A_DQ<42>	MAKE_BASE=TRUE	=MEM_A_DQ<42>	27
79 11	MEM_A_DQ<41>	MAKE_BASE=TRUE	=MEM_A_DQ<40>	27
79 11	MEM_A_DQ<40>	MAKE_BASE=TRUE	=MEM_A_DQ<44>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 6 -> DIMM A DQS 6

79 11	MEM_A_DQS_N<6>	MAKE_BASE=TRUE	=MEM_A_DQS_N<6>	27
79 11	MEM_A_DQS_P<6>	MAKE_BASE=TRUE	=MEM_A_DQS_P<6>	27
		MAKE_BASE=TRUE	=MEM_A_DM<6>	27
79 11	MEM_A_DQ<55>	MAKE_BASE=TRUE	=MEM_A_DQ<51>	27
79 11	MEM_A_DQ<54>	MAKE_BASE=TRUE	=MEM_A_DQ<54>	27
79 11	MEM_A_DQ<53>	MAKE_BASE=TRUE	=MEM_A_DQ<49>	27
79 11	MEM_A_DQ<52>	MAKE_BASE=TRUE	=MEM_A_DQ<53>	27
79 11	MEM_A_DQ<51>	MAKE_BASE=TRUE	=MEM_A_DQ<50>	27
79 11	MEM_A_DQ<50>	MAKE_BASE=TRUE	=MEM_A_DQ<55>	27
79 11	MEM_A_DQ<49>	MAKE_BASE=TRUE	=MEM_A_DQ<48>	27
79 11	MEM_A_DQ<48>	MAKE_BASE=TRUE	=MEM_A_DQ<52>	27
		MAKE_BASE=TRUE		

CPU CHANNEL A DQS 7 -> DIMM A DQS 7

79 11	MEM_A_DQS_N<7>	MAKE_BASE=TRUE	=MEM_A_DQS_N<7>	27
79 11	MEM_A_DQS_P<7>	MAKE_BASE=TRUE	=MEM_A_DQS_P<7>	27
		MAKE_BASE=TRUE	=MEM_A_DM<7>	27
79 11	MEM_A_DQ<63>	MAKE_BASE=TRUE	=MEM_A_DQ<58>	27
79 11	MEM_A_DQ<62>	MAKE_BASE=TRUE	=MEM_A_DQ<59>	27
79 11	MEM_A_DQ<61>	MAKE_BASE=TRUE	=MEM_A_DQ<60>	27
79 11	MEM_A_DQ<60>	MAKE_BASE=TRUE	=MEM_A_DQ<57>	27
79 11	MEM_A_DQ<59>	MAKE_BASE=TRUE	=MEM_A_DQ<63>	27
79 11	MEM_A_DQ<58>	MAKE_BASE=TRUE	=MEM_A_DQ<62>	27
79 11	MEM_A_DQ<57>	MAKE_BASE=TRUE	=MEM_A_DQ<61>	27
79 11	MEM_A_DQ<56>	MAKE_BASE=TRUE	=MEM_A_DQ<56>	27
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 0 -> DIMM B DQS 0

79 11	MEM_B_DQS_N<0>	MAKE_BASE=TRUE	=MEM_B_DQS_N<0>	29
79 11	MEM_B_DQS_P<0>	MAKE_BASE=TRUE	=MEM_B_DQS_P<0>	29
		MAKE_BASE=TRUE	=MEM_B_DM<0>	29
79 11	MEM_B_DQ<7>	MAKE_BASE=TRUE	=MEM_B_DQ<3>	29
79 11	MEM_B_DQ<6>	MAKE_BASE=TRUE	=MEM_B_DQ<2>	29
79 11	MEM_B_DQ<5>	MAKE_BASE=TRUE	=MEM_B_DQ<0>	29
79 11	MEM_B_DQ<4>	MAKE_BASE=TRUE	=MEM_B_DQ<4>	29
79 11	MEM_B_DQ<3>	MAKE_BASE=TRUE	=MEM_B_DQ<7>	29
79 11	MEM_B_DQ<2>	MAKE_BASE=TRUE	=MEM_B_DQ<6>	29
79 11	MEM_B_DQ<1>	MAKE_BASE=TRUE	=MEM_B_DQ<5>	29
79 11	MEM_B_DQ<0>	MAKE_BASE=TRUE	=MEM_B_DQ<1>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 1 -> DIMM B DQS 1

79 11	MEM_B_DQS_N<1>	MAKE_BASE=TRUE	=MEM_B_DQS_N<1>	29
79 11	MEM_B_DQS_P<1>	MAKE_BASE=TRUE	=MEM_B_DQS_P<1>	29
		MAKE_BASE=TRUE	=MEM_B_DM<1>	29
79 11	MEM_B_DQ<15>	MAKE_BASE=TRUE	=MEM_B_DQ<15>	29
79 11	MEM_B_DQ<14>	MAKE_BASE=TRUE	=MEM_B_DQ<14>	29
79 11	MEM_B_DQ<13>	MAKE_BASE=TRUE	=MEM_B_DQ<13>	29
79 11	MEM_B_DQ<12>	MAKE_BASE=TRUE	=MEM_B_DQ<8>	29
79 11	MEM_B_DQ<11>	MAKE_BASE=TRUE	=MEM_B_DQ<11>	29
79 11	MEM_B_DQ<10>	MAKE_BASE=TRUE	=MEM_B_DQ<10>	29
79 11	MEM_B_DQ<9>	MAKE_BASE=TRUE	=MEM_B_DQ<12>	29
79 11	MEM_B_DQ<8>	MAKE_BASE=TRUE	=MEM_B_DQ<9>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 2 -> DIMM B DQS 2

79 11	MEM_B_DQS_N<2>	MAKE_BASE=TRUE	=MEM_B_DQS_N<2>	29
79 11	MEM_B_DQS_P<2>	MAKE_BASE=TRUE	=MEM_B_DQS_P<2>	29
		MAKE_BASE=TRUE	=MEM_B_DM<2>	29
79 11	MEM_B_DQ<23>	MAKE_BASE=TRUE	=MEM_B_DQ<23>	29
79 11	MEM_B_DQ<22>	MAKE_BASE=TRUE	=MEM_B_DQ<18>	29
79 11	MEM_B_DQ<21>	MAKE_BASE=TRUE	=MEM_B_DQ<16>	29
79 11	MEM_B_DQ<20>	MAKE_BASE=TRUE	=MEM_B_DQ<17>	29
79 11	MEM_B_DQ<19>	MAKE_BASE=TRUE	=MEM_B_DQ<22>	29
79 11	MEM_B_DQ<18>	MAKE_BASE=TRUE	=MEM_B_DQ<19>	29
79 11	MEM_B_DQ<17>	MAKE_BASE=TRUE	=MEM_B_DQ<21>	29
79 11	MEM_B_DQ<16>	MAKE_BASE=TRUE	=MEM_B_DQ<20>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 3 -> DIMM B DQS 3

79 11	MEM_B_DQS_N<3>	MAKE_BASE=TRUE	=MEM_B_DQS_N<3>	29
79 11	MEM_B_DQS_P<3>	MAKE_BASE=TRUE	=MEM_B_DQS_P<3>	29
		MAKE_BASE=TRUE	=MEM_B_DM<3>	29
79 11	MEM_B_DQ<31>	MAKE_BASE=TRUE	=MEM_B_DQ<26>	29
79 11	MEM_B_DQ<30>	MAKE_BASE=TRUE	=MEM_B_DQ<30>	29
79 11	MEM_B_DQ<29>	MAKE_BASE=TRUE	=MEM_B_DQ<28>	29
79 11	MEM_B_DQ<28>	MAKE_BASE=TRUE	=MEM_B_DQ<29>	29
79 11	MEM_B_DQ<27>	MAKE_BASE=TRUE	=MEM_B_DQ<27>	29
79 11	MEM_B_DQ<26>	MAKE_BASE=TRUE	=MEM_B_DQ<31>	29
79 11	MEM_B_DQ<25>	MAKE_BASE=TRUE	=MEM_B_DQ<25>	29
79 11	MEM_B_DQ<24>	MAKE_BASE=TRUE	=MEM_B_DQ<24>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 4 -> DIMM B DQS 4

79 11	MEM_B_DQS_N<4>	MAKE_BASE=TRUE	=MEM_B_DQS_N<4>	29
79 11	MEM_B_DQS_P<4>	MAKE_BASE=TRUE	=MEM_B_DQS_P<4>	29
		MAKE_BASE=TRUE	=MEM_B_DM<4>	29
79 11	MEM_B_DQ<39>	MAKE_BASE=TRUE	=MEM_B_DQ<38>	29
79 11	MEM_B_DQ<38>	MAKE_BASE=TRUE	=MEM_B_DQ<39>	29
79 11	MEM_B_DQ<37>	MAKE_BASE=TRUE	=MEM_B_DQ<33>	29
79 11	MEM_B_DQ<36>	MAKE_BASE=TRUE	=MEM_B_DQ<37>	29
79 11	MEM_B_DQ<35>	MAKE_BASE=TRUE	=MEM_B_DQ<34>	29
79 11	MEM_B_DQ<34>	MAKE_BASE=TRUE	=MEM_B_DQ<35>	29
79 11	MEM_B_DQ<33>	MAKE_BASE=TRUE	=MEM_B_DQ<32>	29
79 11	MEM_B_DQ<32>	MAKE_BASE=TRUE	=MEM_B_DQ<36>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 5 -> DIMM B DQS 5

79 11	MEM_B_DQS_N<5>	MAKE_BASE=TRUE	=MEM_B_DQS_N<5>	29
79 11	MEM_B_DQS_P<5>	MAKE_BASE=TRUE	=MEM_B_DQS_P<5>	29
		MAKE_BASE=TRUE	=MEM_B_DM<5>	29
79 11	MEM_B_DQ<47>	MAKE_BASE=TRUE	=MEM_B_DQ<43>	29
79 11	MEM_B_DQ<46>	MAKE_BASE=TRUE	=MEM_B_DQ<46>	29
79 11	MEM_B_DQ<45>	MAKE_BASE=TRUE	=MEM_B_DQ<40>	29
79 11	MEM_B_DQ<44>	MAKE_BASE=TRUE	=MEM_B_DQ<45>	29
79 11	MEM_B_DQ<43>	MAKE_BASE=TRUE	=MEM_B_DQ<47>	29
79 11	MEM_B_DQ<42>	MAKE_BASE=TRUE	=MEM_B_DQ<42>	29
79 11	MEM_B_DQ<41>	MAKE_BASE=TRUE	=MEM_B_DQ<41>	29
79 11	MEM_B_DQ<40>	MAKE_BASE=TRUE	=MEM_B_DQ<44>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 6 -> DIMM B DQS 6

79 11	MEM_B_DQS_N<6>	MAKE_BASE=TRUE	=MEM_B_DQS_N<6>	29
79 11	MEM_B_DQS_P<6>	MAKE_BASE=TRUE	=MEM_B_DQS_P<6>	29
		MAKE_BASE=TRUE	=MEM_B_DM<6>	29
79 11	MEM_B_DQ<55>	MAKE_BASE=TRUE	=MEM_B_DQ<54>	29
79 11	MEM_B_DQ<54>	MAKE_BASE=TRUE	=MEM_B_DQ<55>	29
79 11	MEM_B_DQ<53>	MAKE_BASE=TRUE	=MEM_B_DQ<53>	29
79 11	MEM_B_DQ<52>	MAKE_BASE=TRUE	=MEM_B_DQ<49>	29
79 11	MEM_B_DQ<51>	MAKE_BASE=TRUE	=MEM_B_DQ<51>	29
79 11	MEM_B_DQ<50>	MAKE_BASE=TRUE	=MEM_B_DQ<50>	29
79 11	MEM_B_DQ<49>	MAKE_BASE=TRUE	=MEM_B_DQ<48>	29
79 11	MEM_B_DQ<48>	MAKE_BASE=TRUE	=MEM_B_DQ<52>	29
		MAKE_BASE=TRUE		

CPU CHANNEL B DQS 7 -> DIMM B DQS 7

79 11	MEM_B_DQS_N<7>	MAKE_BASE=TRUE	=MEM_B_DQS_N<7>	29
79 11	MEM_B_DQS_P<7>	MAKE_BASE=TRUE	=MEM_B_DQS_P<7>	29
		MAKE_BASE=TRUE	=MEM_B_DM<7>	29
79 11	MEM_B_DQ<63>	MAKE_BASE=TRUE	=MEM_B_DQ<56>	29
79 11	MEM_B_DQ<62>	MAKE_BASE=TRUE	=MEM_B_DQ<59>	29
79 11	MEM_B_DQ<61>	MAKE_BASE=TRUE	=MEM_B_DQ<61>	29
79 11	MEM_B_DQ<60>	MAKE_BASE=TRUE	=MEM_B_DQ<60>	29
79 11	MEM_B_DQ<59>	MAKE_BASE=TRUE	=MEM_B_DQ<63>	29
79 11	MEM_B_DQ<58>	MAKE_BASE=TRUE	=MEM_B_DQ<58>	29
79 11	MEM_B_DQ<57>	MAKE_BASE=TRUE	=MEM_B_DQ<57>	29
79 11	MEM_B_DQ<56>	MAKE_BASE=TRUE	=MEM_B_DQ<62>	29
		MAKE_BASE=TRUE		

NOTE: Ivybridge does not use DM signals per doc 460452 CR SFF DG Section 2.6.14

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE
DDR3 Byte/Bit Swaps

Apple Inc.

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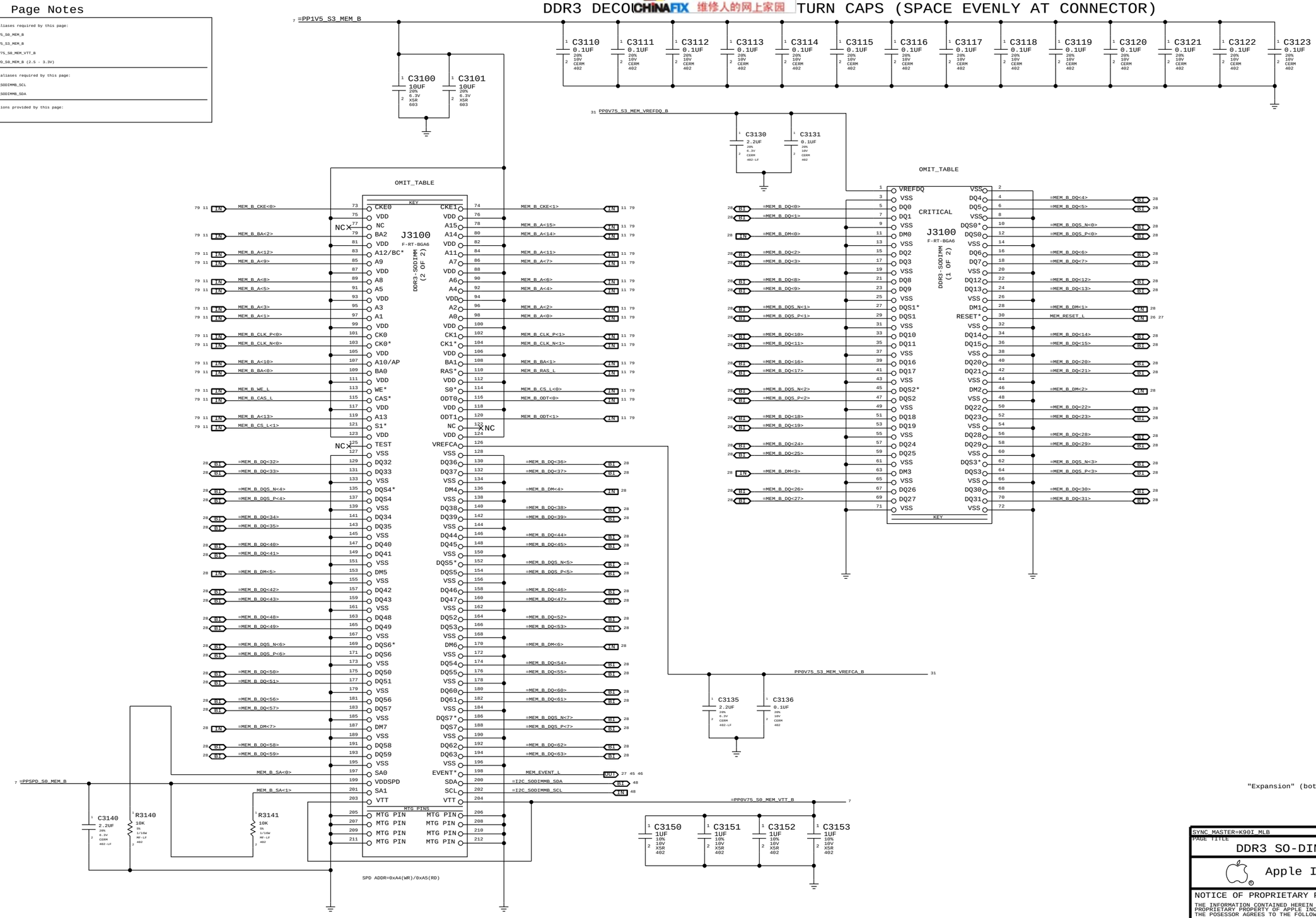
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PPSPD_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING RETURN CAPS (SPACE EVENLY AT CONNECTOR)



"Expansion" (bottom) slot

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE: DDR3 SO-DIMM Connector B

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

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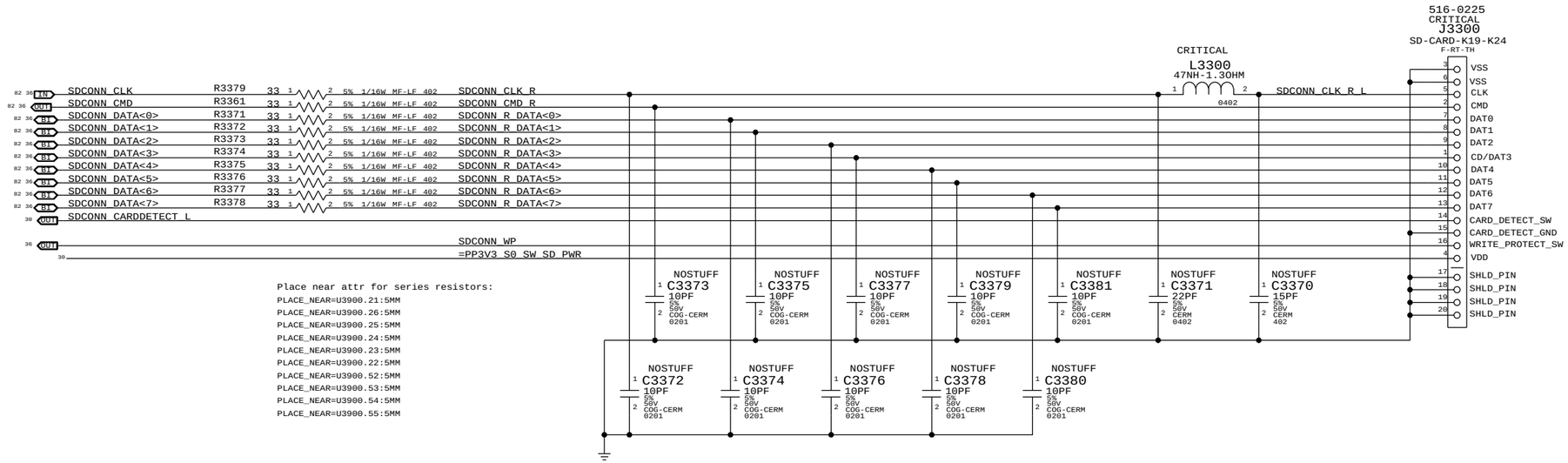
SD Card Connector

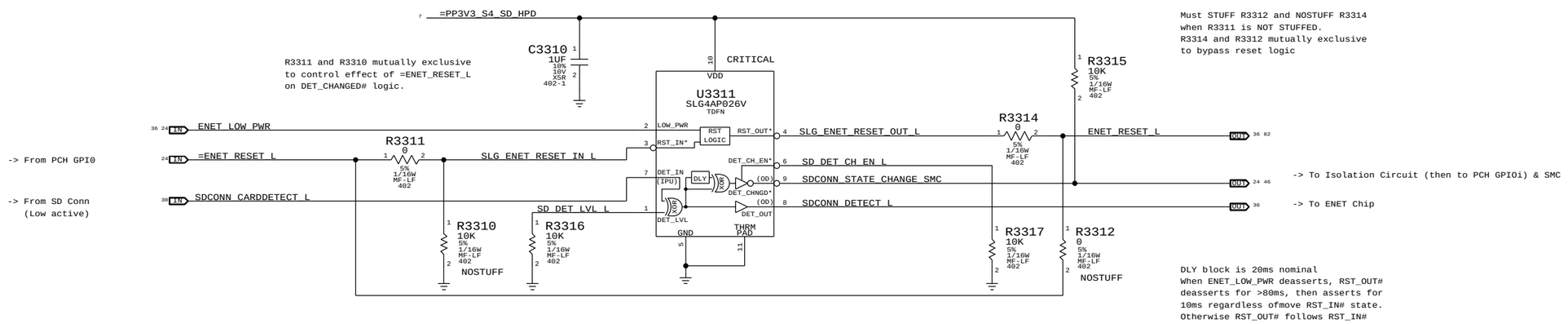


Place near attr for series resistors:
PLACE_NEAR=U3900.21:5MM
PLACE_NEAR=U3900.26:5MM
PLACE_NEAR=U3900.25:5MM
PLACE_NEAR=U3900.24:5MM
PLACE_NEAR=U3900.23:5MM
PLACE_NEAR=U3900.22:5MM
PLACE_NEAR=U3900.52:5MM
PLACE_NEAR=U3900.53:5MM
PLACE_NEAR=U3900.54:5MM
PLACE_NEAR=U3900.55:5MM

SD Not Inserted, CARD_DETECT is OPEN.
CAESAR-IV Card Detect is programmable,
but a Silicon bug makes the active
high case unusable.

SD Detect & Reset Logic

SDCONN_DETECT Debounce, Inversion, Detect-Changed PCH GPIO Latch Circuit
Converts SDCONN from active-low level signal to active-high pulses.



-> From PCH GPI0

-> From SD Conn
(Low active)

R3311 and R3310 mutually exclusive
to control effect of =ENET_RESET_L
on DET_CHANGED# logic.

Must STUFF R3312 and NOSTUFF R3314
when R3311 is NOT STUFFED.
R3314 and R3312 mutually exclusive
to bypass reset logic

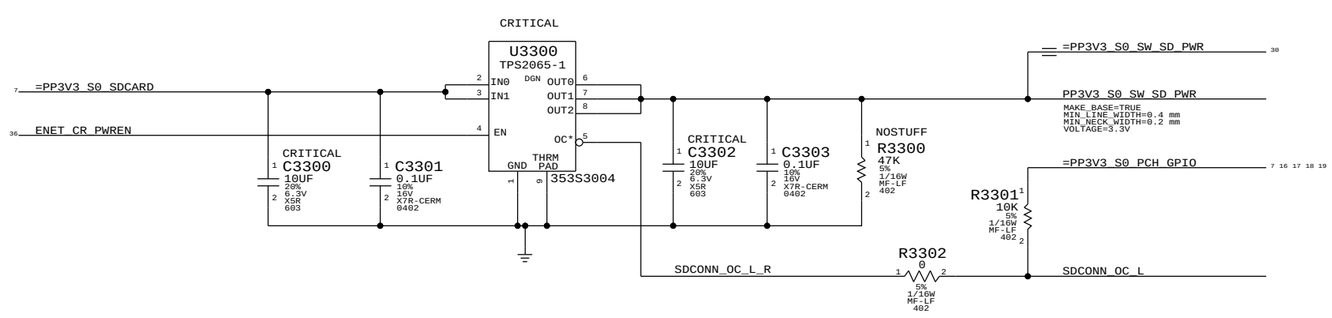
-> To Isolation Circuit (then to PCH GPIOi) & SMC

-> To ENET Chip

DLY block is 20ms nominal
When ENET_LOW_PWR deasserts, RST_OUT#
deasserts for >80ms, then asserts for
10ms regardless ofmove RST_IN# state.
Otherwise RST_OUT# follows RST_IN#

SD Card 3.3V Overcurrent Protection

TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



SYNC_MASTER=YONAS_J30	SYNC_DATE=11/03/2011
PAGE TITLE: SD Card Connector	
Apple Inc.	DRAWING NUMBER: 051-9058 SIZE: D
	REVISION: 6.0.0
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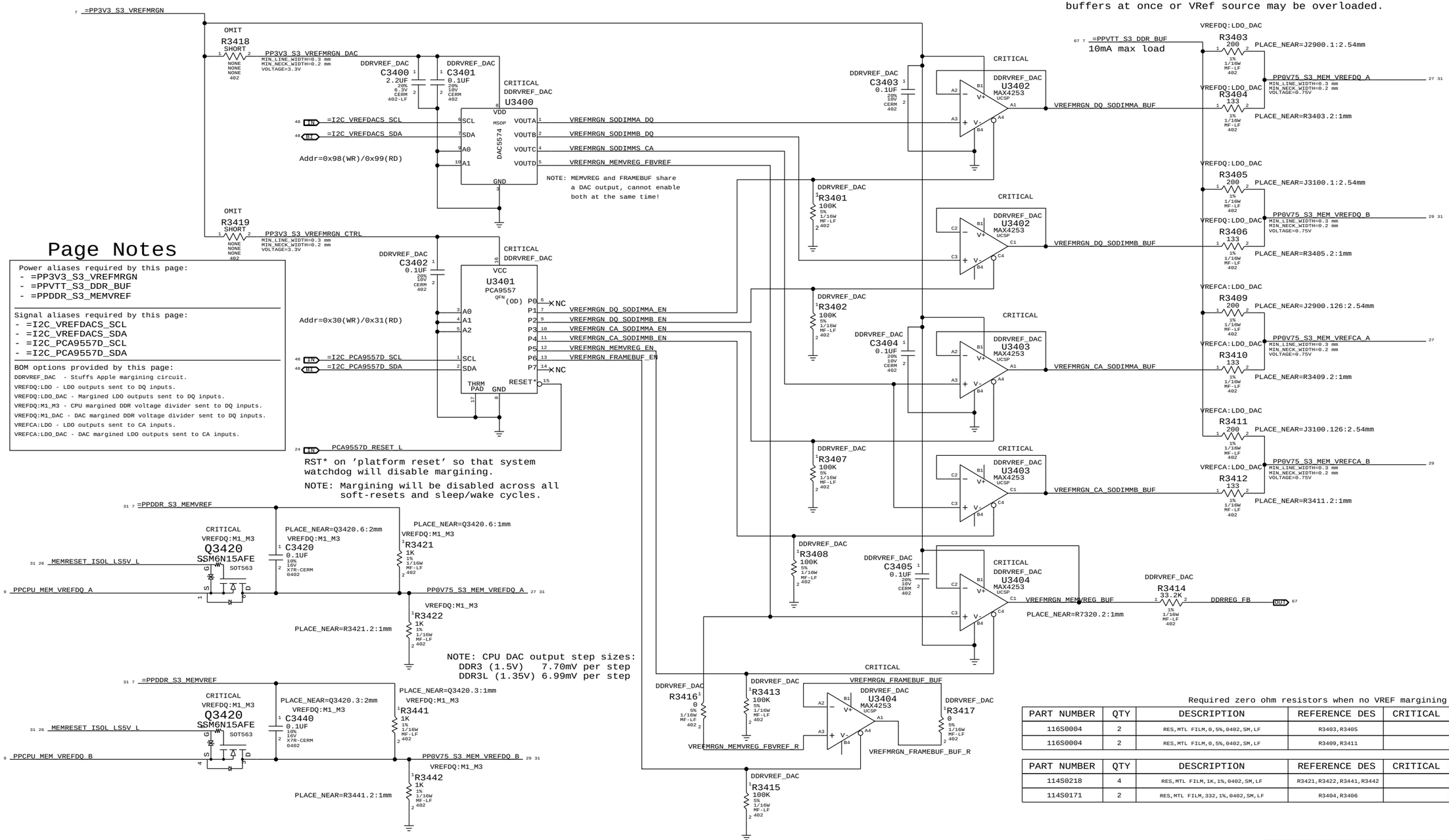
NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
DDRVREF_DAC - Stuffs Apple margining circuit.
VREFDQ:LDO - LDO outputs sent to DQ inputs.
VREFDQ:LDO_DAC - Margined LDO outputs sent to DQ inputs.
VREFDQ:M1_M3 - CPU margined DDR voltage divider sent to DQ inputs.
VREFDQ:M1_DAC - DAC margined DDR voltage divider sent to DQ inputs.
VREFCA:LDO - LDO outputs sent to CA inputs.
VREFCA:LDO_DAC - DAC margined LDO outputs sent to CA inputs.

Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3403,R3405		VREFDQ:LDO
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3409,R3411		VREFCA:LDO

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0218	4	RES,MTL FILM,1K,1%,0402,SM,LF	R3421,R3422,R3441,R3442		VREFDQ:M1_DAC
114S0171	2	RES,MTL FILM,332,1%,0402,SM,LF	R3404,R3406		VREFDQ:M1_DAC

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.000V - 2.000V (+/- 500mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 3.000V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+61uA - -61uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=J31 MLB SYNC DATE=06/13/2011

PAGE TITLE
DDR3/FRAMEBUF VREF MARGINING

Apple Inc.

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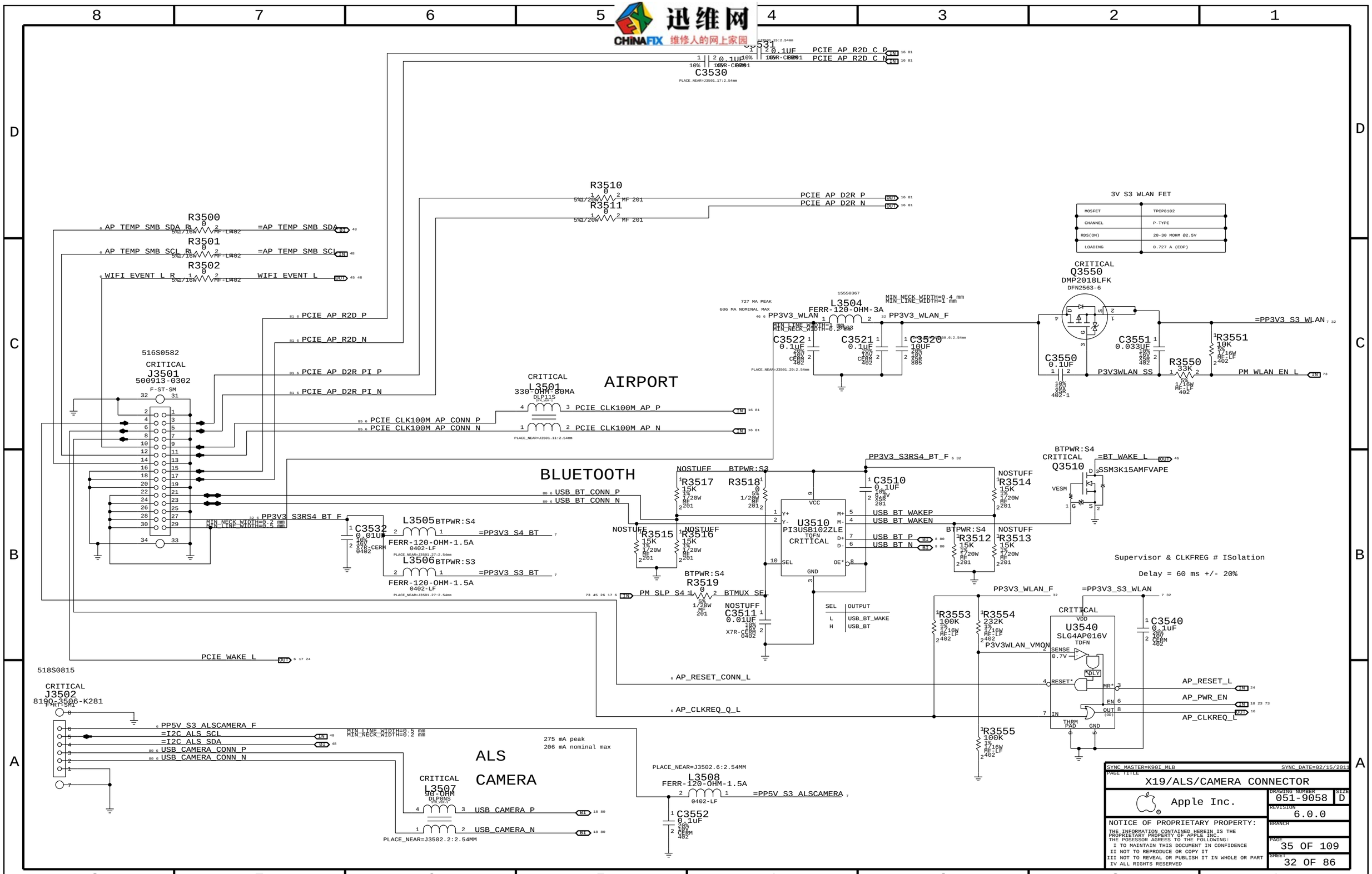
AIRPORT
BLUETOOTH
ALS
CAMERA
J3501
500913-0302
F-ST-SM
516S0582
CRITICAL
J3502
8190-3506-K281
FRT-SM1
518S0815
R3500
R3501
R3502
R3510
R3511
C3530
C3531
PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N
PCIE_AP_R2D_P
PCIE_AP_R2D_N
PCIE_AP_D2R_PI_P
PCIE_AP_D2R_PI_N
PCIE_CLK100M_AP_CONN_P
PCIE_CLK100M_AP_CONN_N
PCIE_AP_D2R_P
PCIE_AP_D2R_N
L3501
330-OHM-80MA
DLP11S
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N
USB_BT_CONN_P
USB_BT_CONN_N
PP3V3_S3RS4_BT_F
C3532
0.01UF
L3505
L3506
FERR-120-OHM-1.5A
=PP3V3_S4_BT
=PP3V3_S3_BT
PCIE_WAKE_L
PP5V_S3_ALSCAMERA_F
=I2C_ALS_SCL
=I2C_ALS_SDA
USB_CAMERA_CONN_P
USB_CAMERA_CONN_N
L3507
90-OHM
DLP6NS
USB_CAMERA_P
USB_CAMERA_N
L3508
=PP5V_S3_ALSCAMERA
C3552
0.1UF
L3504
FERR-120-OHM-3A
PP3V3_WLAN
PP3V3_WLAN_F
C3522
C3521
C3520
10UF
3V S3 WLAN FET
MOSFET
TPCP8102
CHANNEL
P-TYPE
RDS(ON)
20-30 MOHM @2.5V
LOADING
0.727 A (EDP)
Q3550
DMP2018LFK
DFN2563-6
C3550
0.1UF
C3551
0.033UF
R3550
33K
R3551
10K
=PP3V3_S3_WLAN
P3V3WLAN_SS
PM_WLAN_EN_L
BTPWR:S4
Q3510
SSM3K15AMFVAPE
=BT_WAKE_L
VESM
C3510
0.1UF
R3517
15K
R3518
R3515
R3516
R3519
PM_SLP_S4_L
BTMUX_SE
C3511
0.01UF
U3510
PI3USB102ZLE
TDFN
VCC
GND
SEL
USB_BT_WAKEP
USB_BT_WAKEN
USB_BT_P
USB_BT_N
R3512
R3513
R3514
Supervisor & CLKFREG # ISolation
Delay = 60 ms +/- 20%
PP3V3_WLAN_F
=PP3V3_S3_WLAN
R3553
100K
R3554
232K
P3V3WLAN_VMON
U3540
SLG4AP016V
TDFN
C3540
0.1UF
AP_RESET_CONN_L
AP_CLKREQ_Q_L
AP_RESET_L
AP_PWR_EN
AP_CLKREQ_L
R3555
100K
SYNC_MASTER=K90I_MLB
SYNC_DATE=02/15/2011
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X19/ALS/CAMERA CONNECTOR
Apple Inc.
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051-9058
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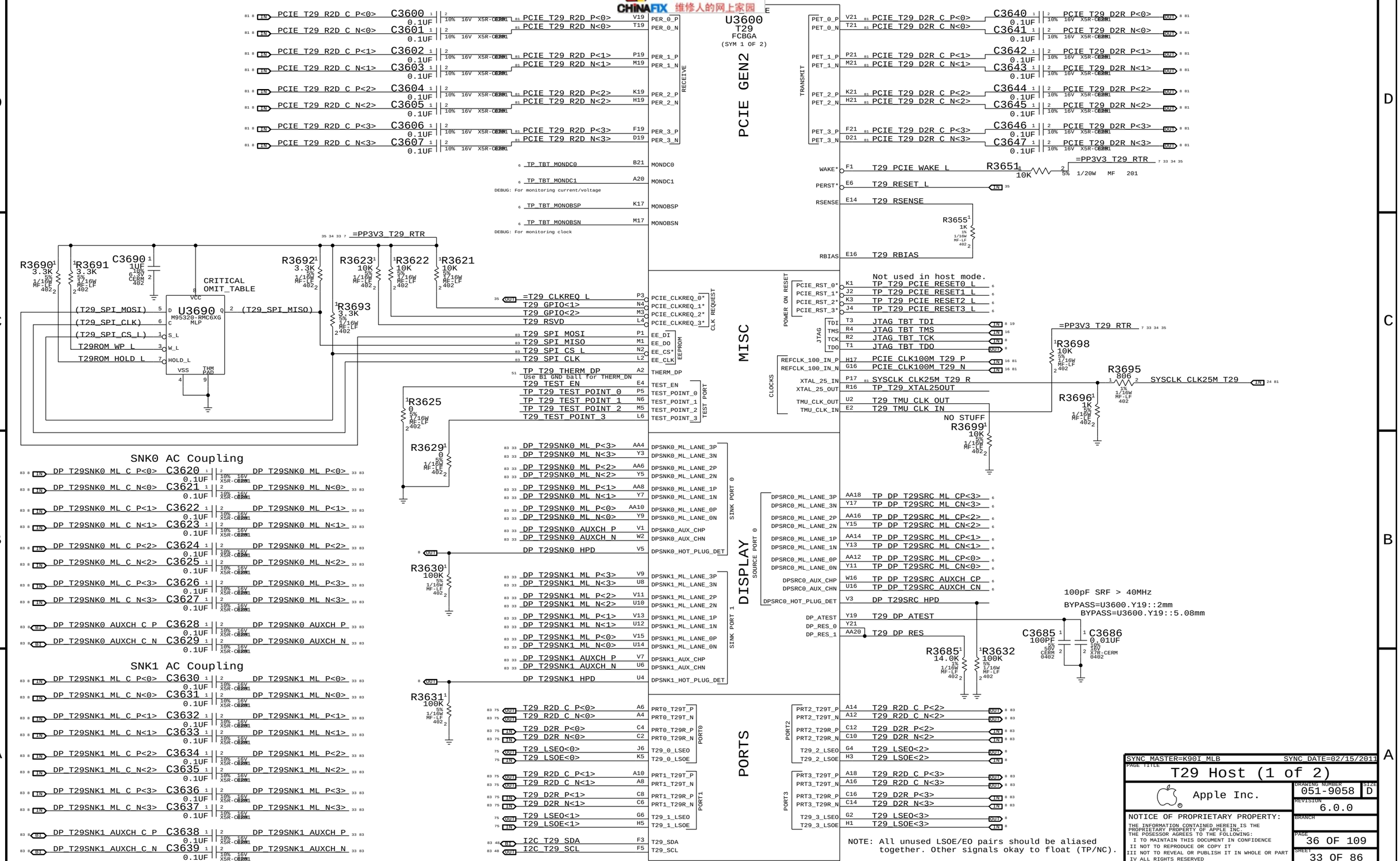

SYNC MASTER=K90I MLB SYNC DATE=02/15/2011

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T29 Host (1 of 2)

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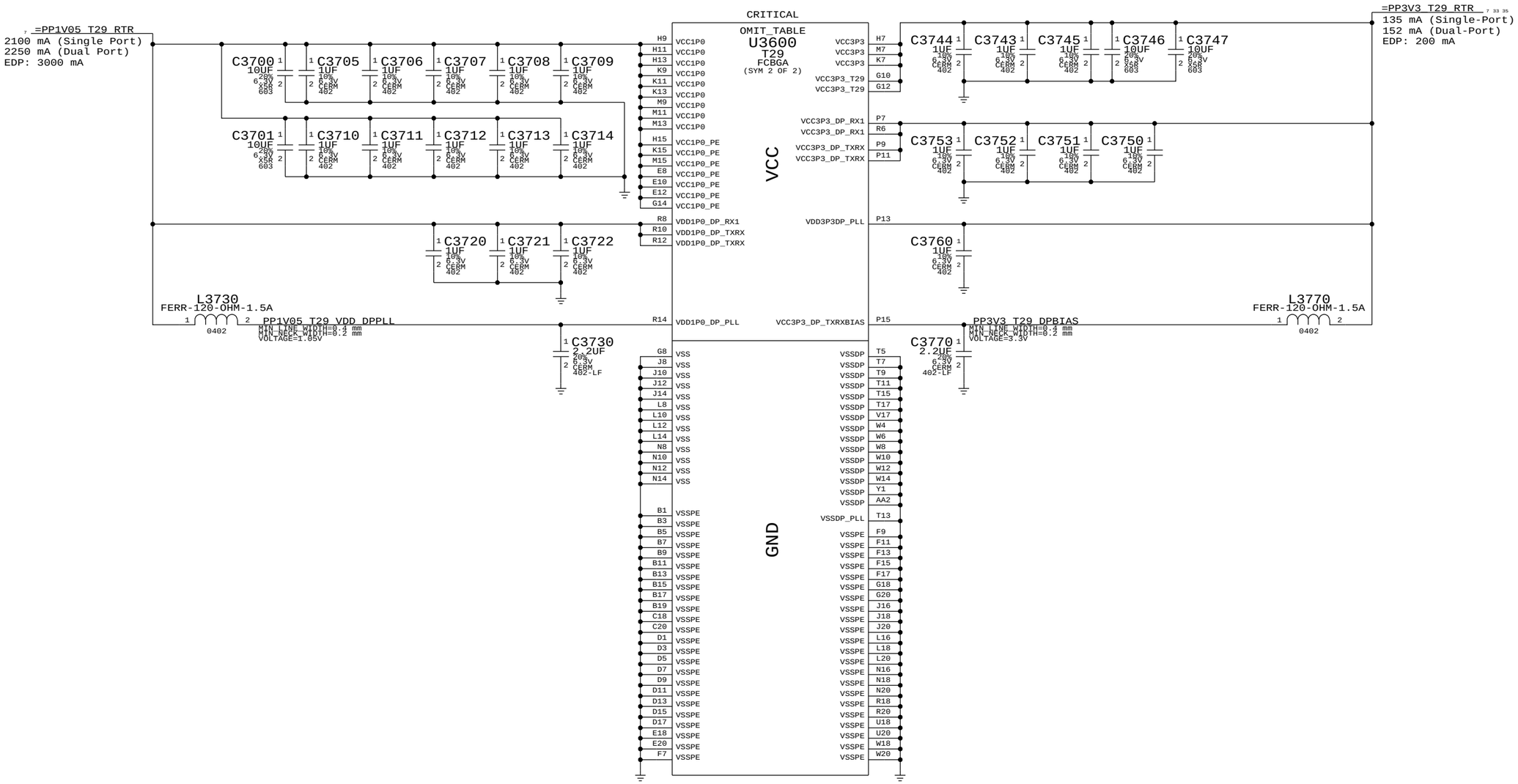

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

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T29 Host (2 of 2)

Apple Inc.

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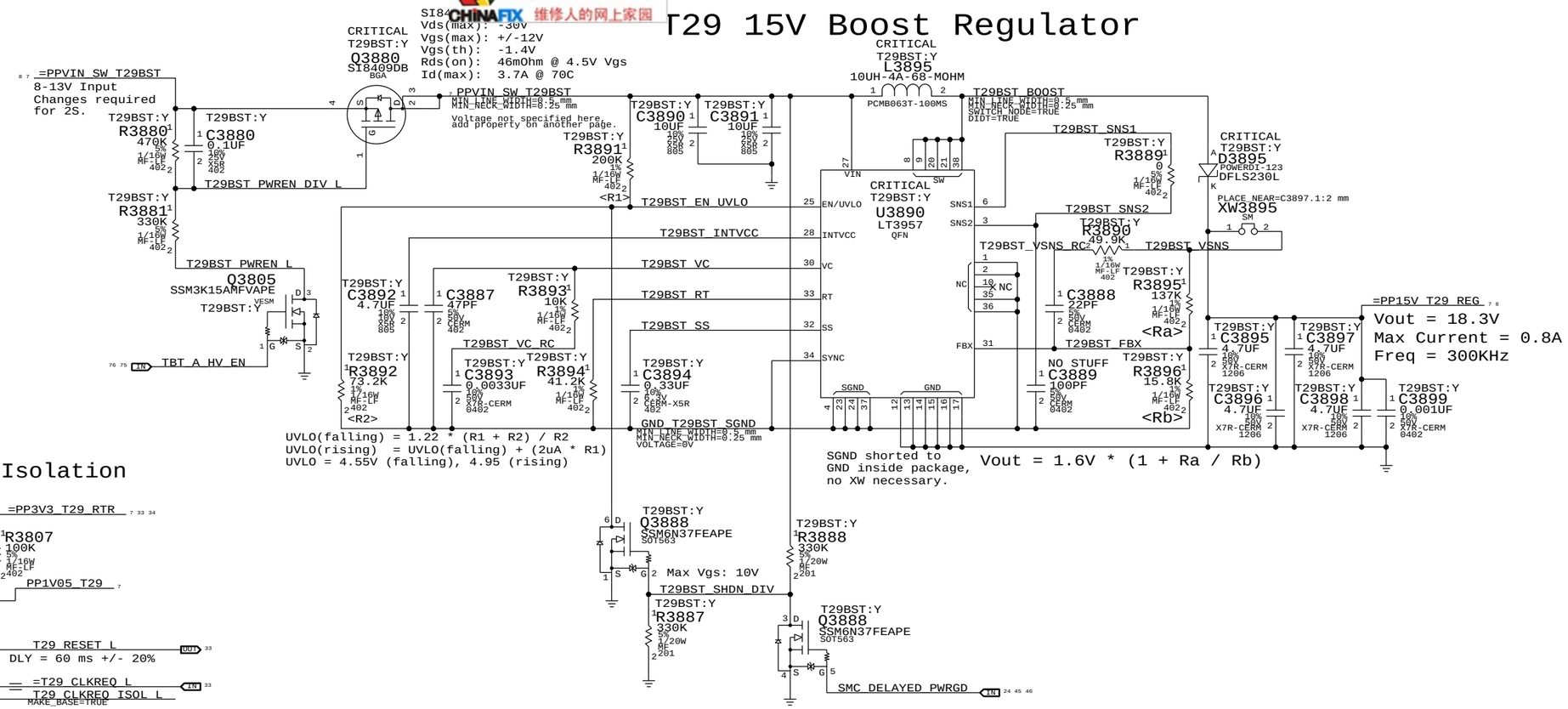
Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

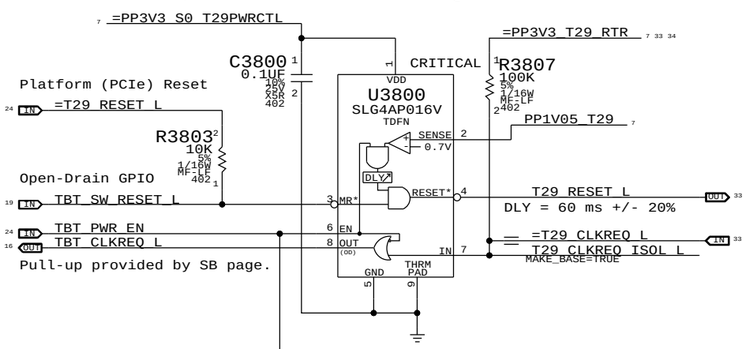
Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

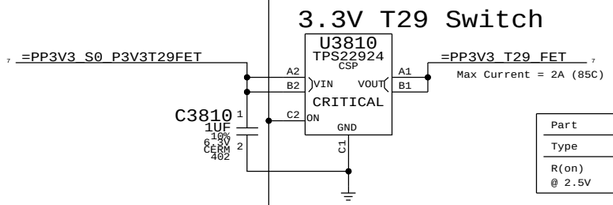
T29 15V Boost Regulator



Supervisor & CLKREQ# Isolation



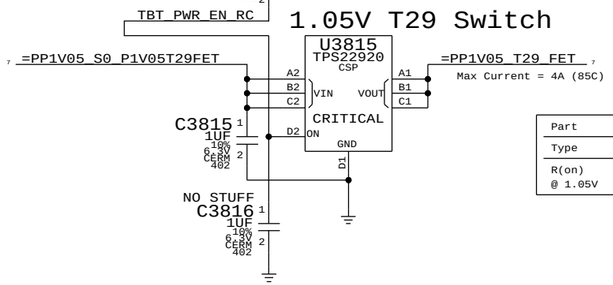
3.3V T29 Switch



U3810

Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.3 mOhm Typ 24 mOhm Max

1.05V T29 Switch



U3815

Part	TPS22920
Type	Load Switch
R(on) @ 1.05V	8 mOhm Typ 11.5 mOhm Max

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011

PAGE TITLE
T29 Power Support

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

REVISION 6.0.0

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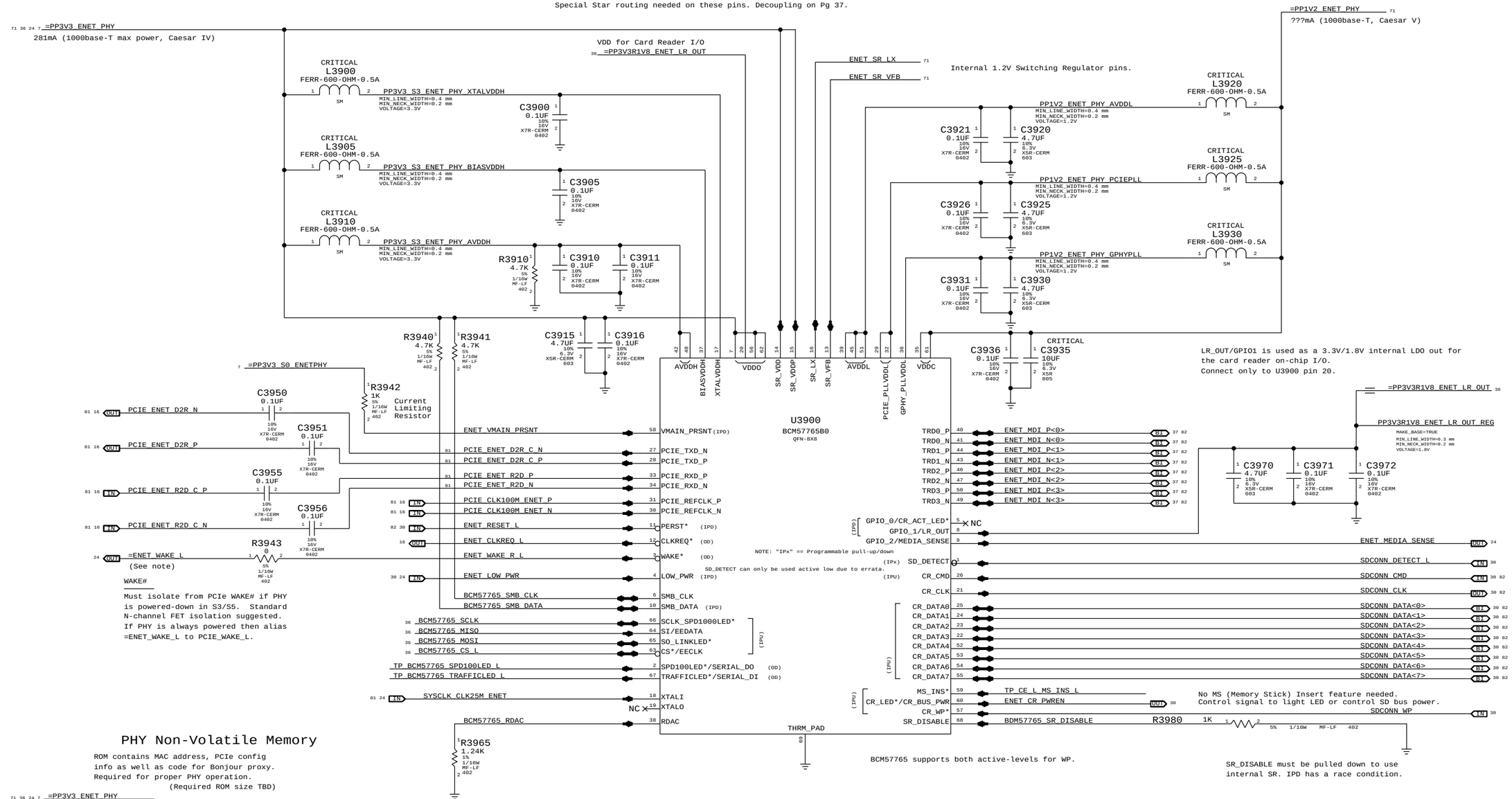
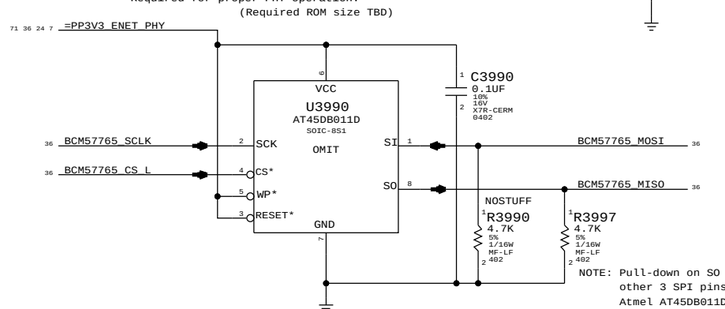
BCM57765 ENET SR pins are internal 1.2V S[illegible]DISABLE below.
If disabled: Okay to float VDD, VDDP & L[illegible]V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.



PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)



NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=J31_MLB SYNC_DATE=06/15/2013

PAGE TITLE
ETHERNET PHY (CAESAR IV)

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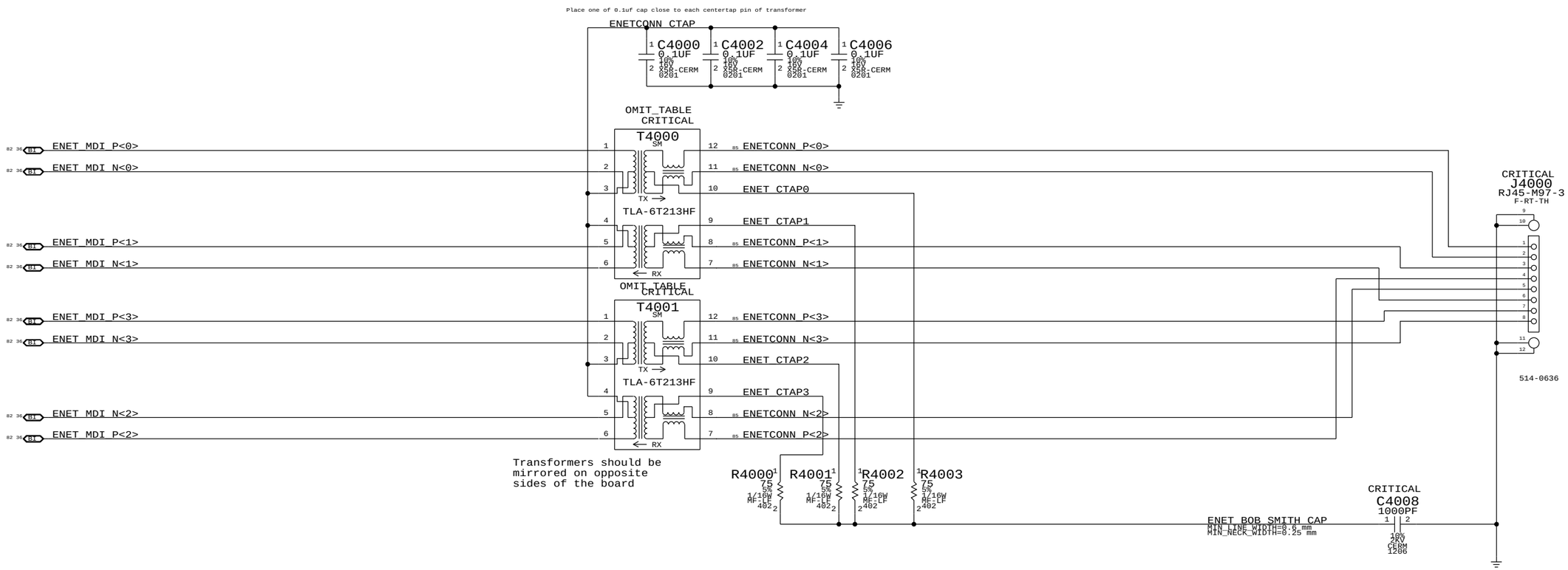
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
157S0084	2	XFMR,ISO,HALF-PORT,1000T,12P,SMD,HF	T4000,T4001	CRITICAL	

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2013

PAGE TITLE
Ethernet Connector

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DRAWING NUMBER 051-9058 SIZE D
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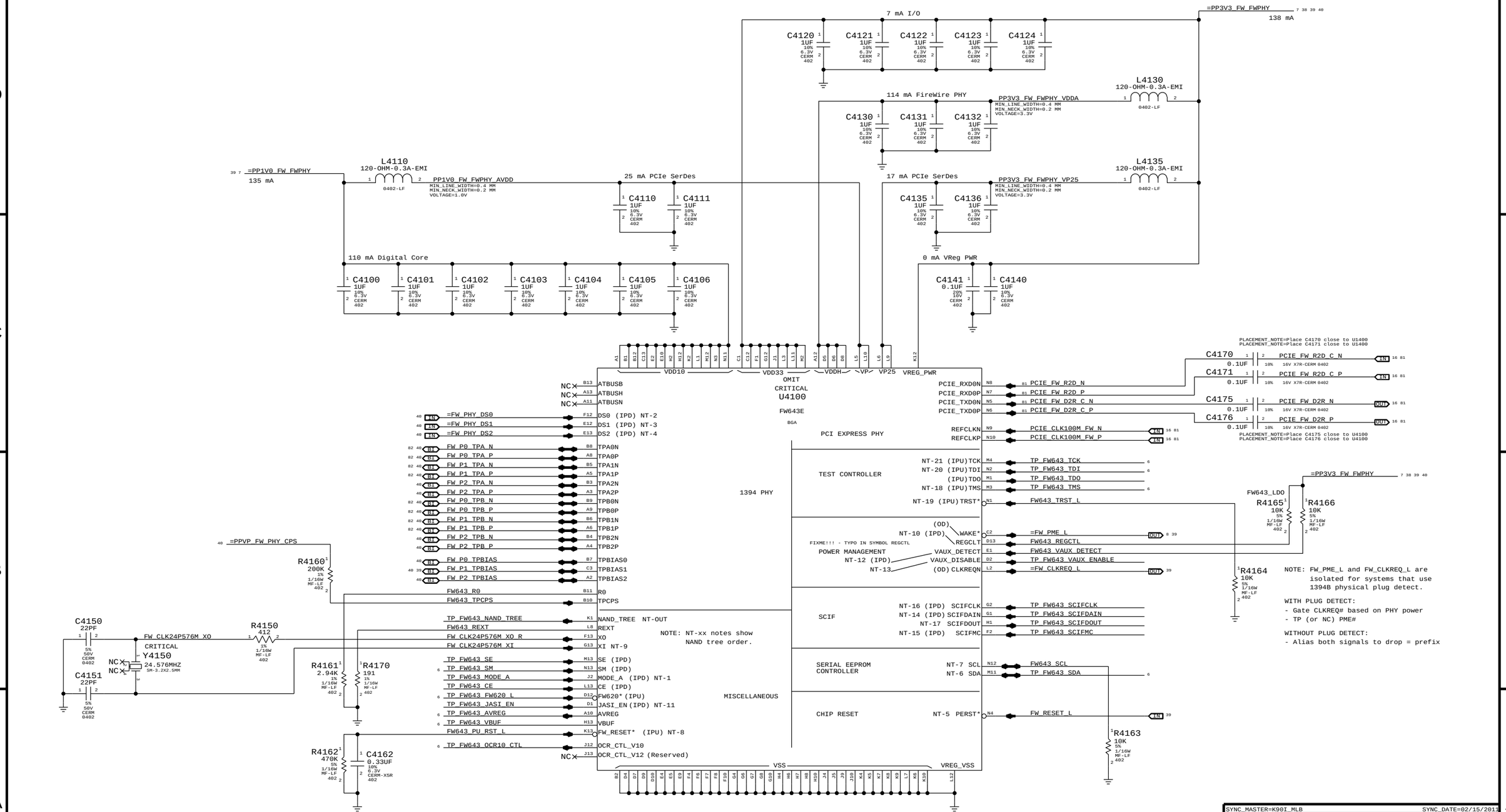

SYNC MASTER=K90I_MLB SYNC_DATE=02/15/2013

PAGE TITLE

FireWire LLC/PHY (FW643E)

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

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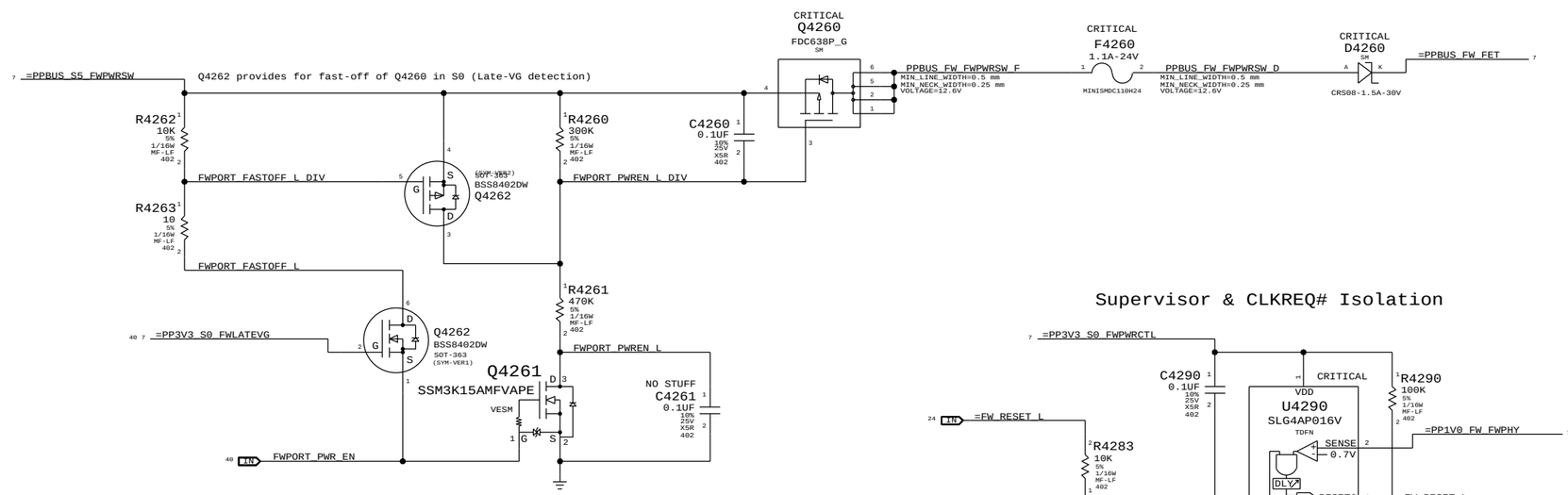
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

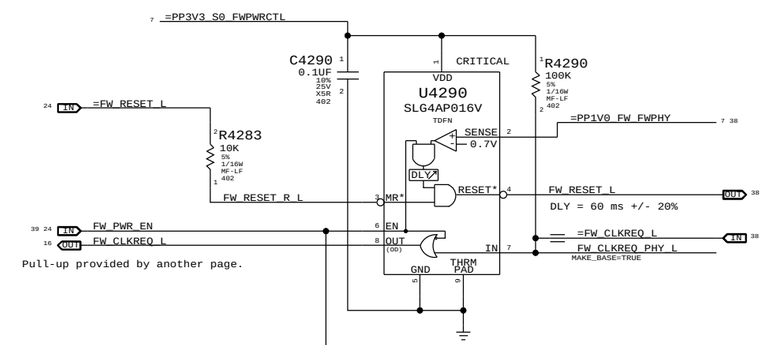
Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

FireWire Port Power Switch

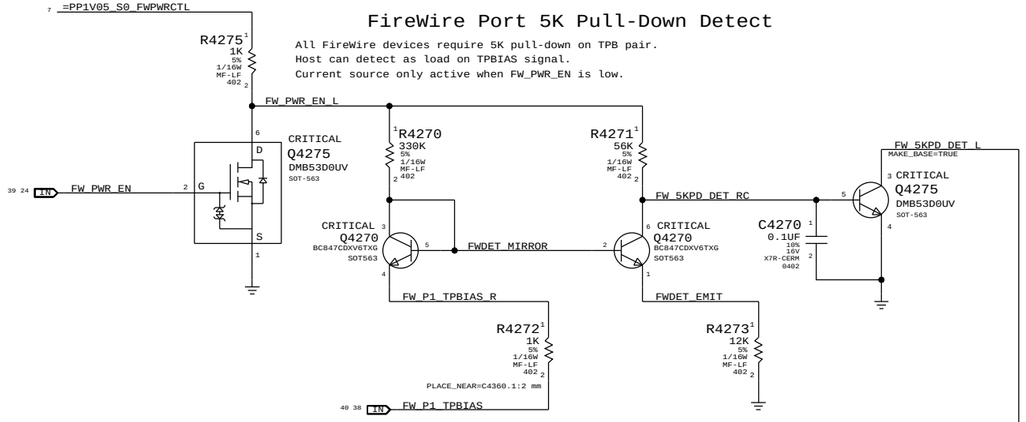


Supervisor & CLKREQ# Isolation



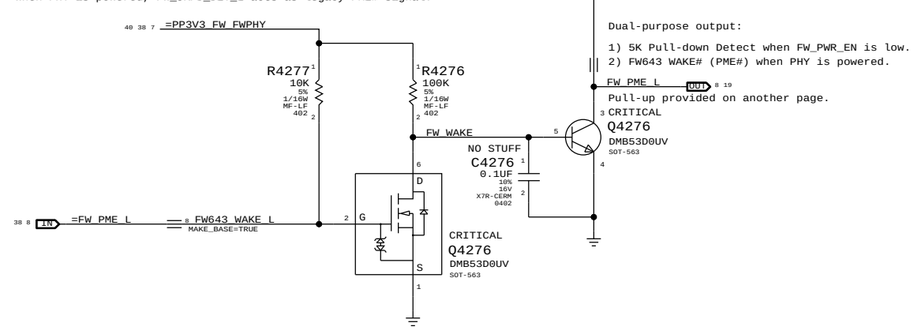
FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.

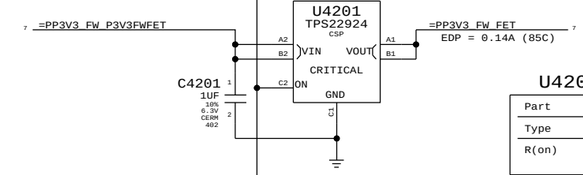


FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.



3.3V FW Switch

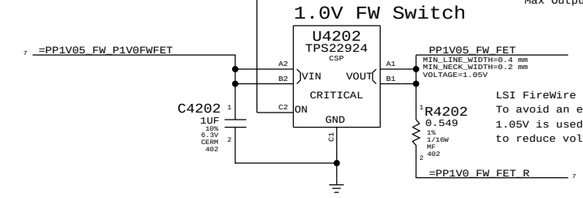


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

1.0V FW Switch



LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC_MASTER=K90I_MLB SYNC_DATE=06/23/2011

PAGE TITLE: FireWire Port & PHY Power

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

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SHEET: 39 OF 86

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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

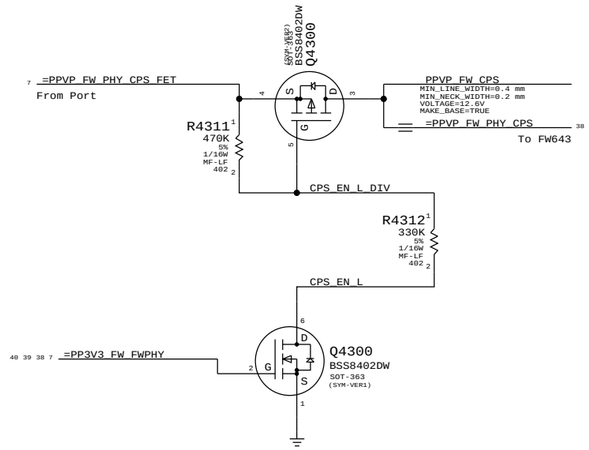
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

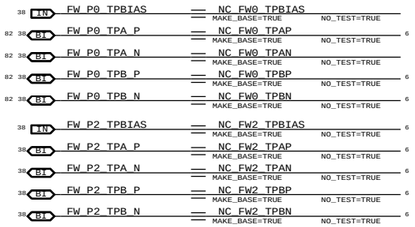
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



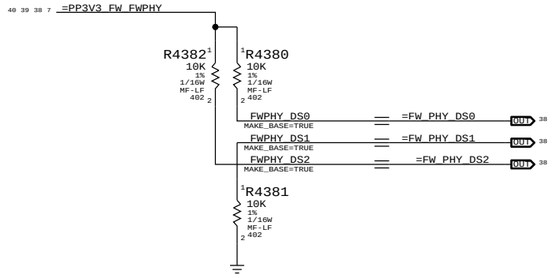
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



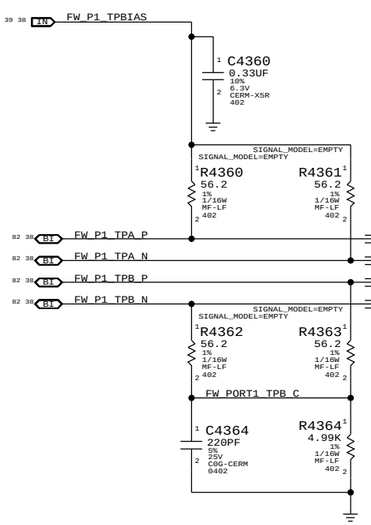
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

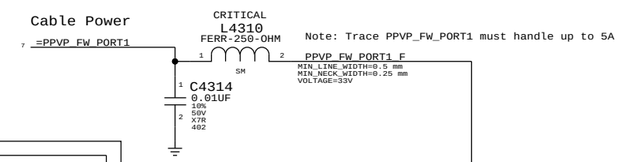


Termination

Place close to FireWire PHY

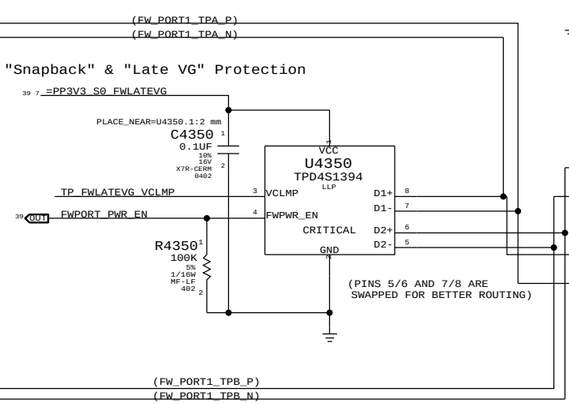


Cable Power



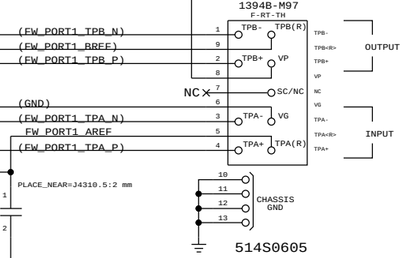
Note: Trace PPVP_FW_PORT1 must handle up to 5A

"Snapback" & "Late VG" Protection



PORT 1

BILINGUAL



AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE: FireWire Connector

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DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

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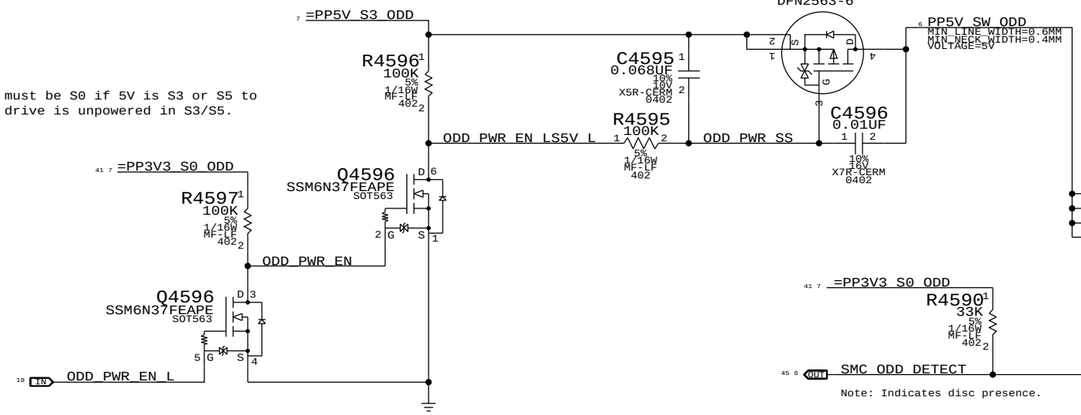
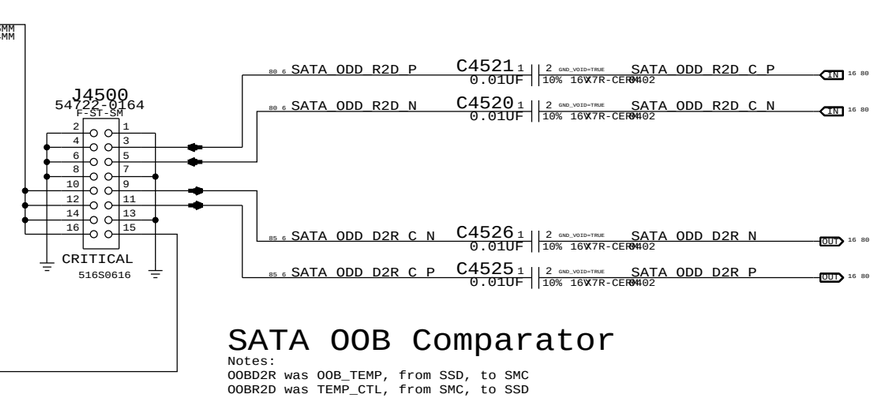
ODD Power Control

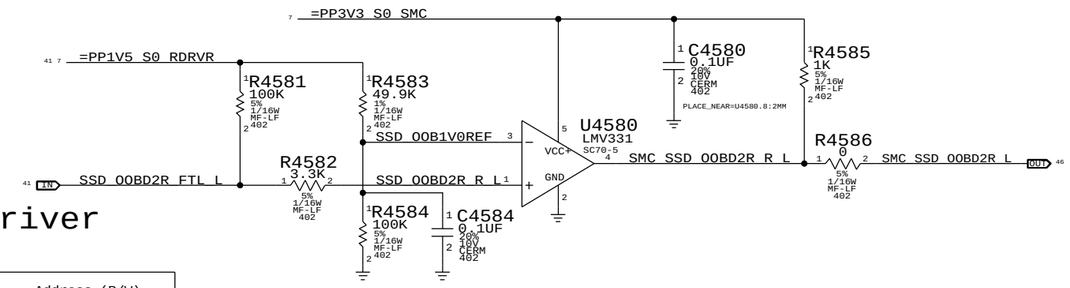


SATA ODD Connector

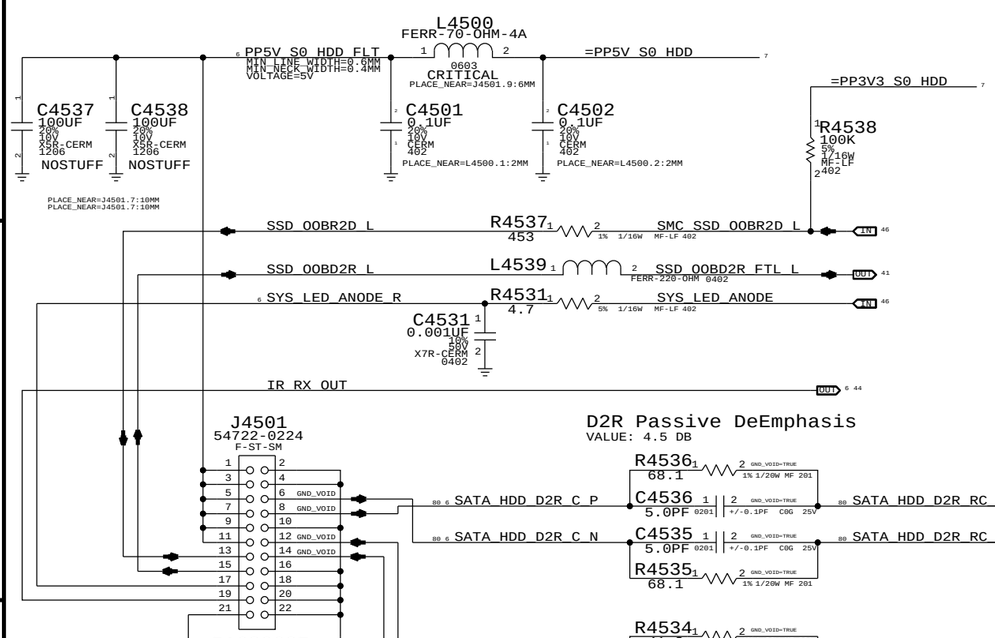


SATA OOB Comparator

Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD



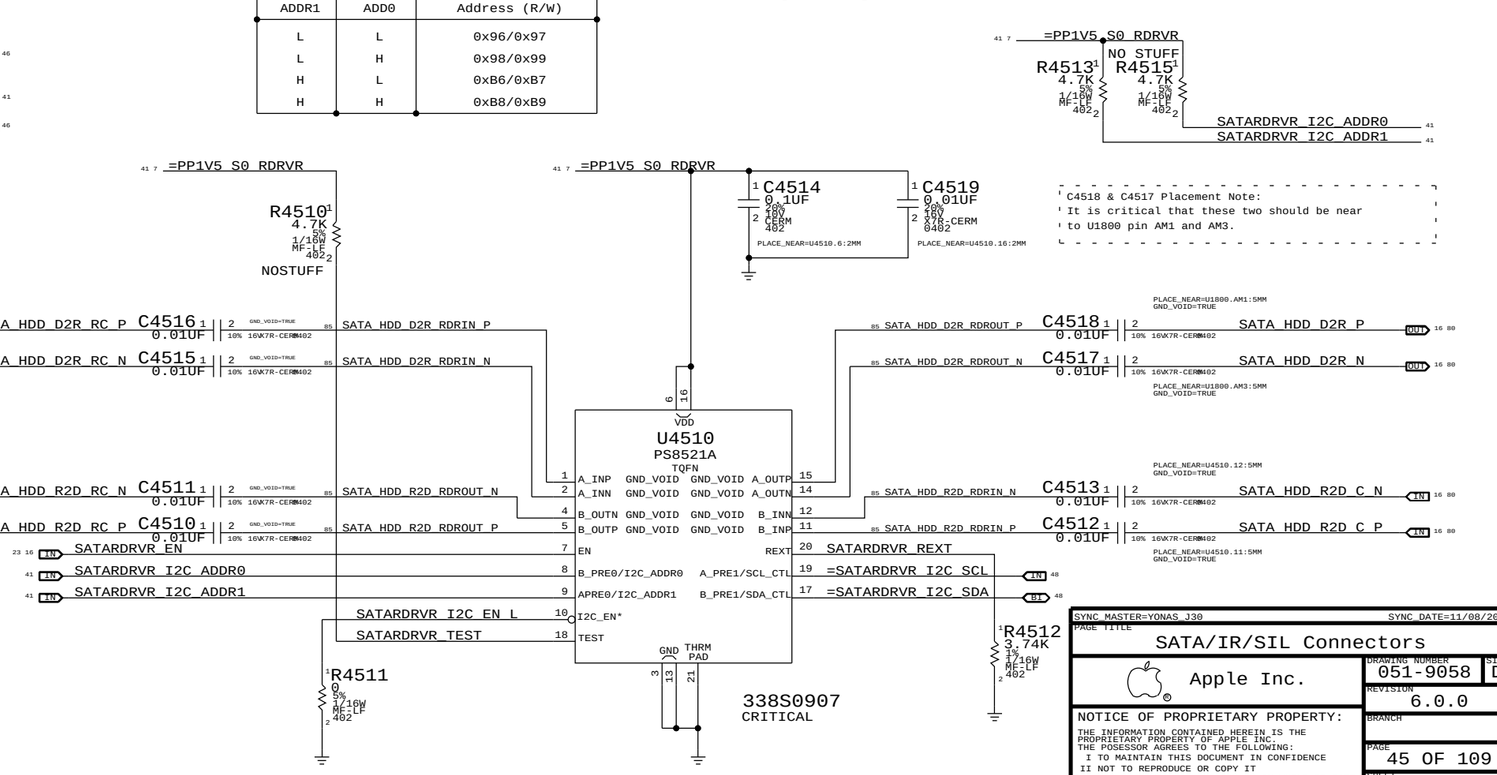
SATA HDD Connector (Gen3)



SATA Redriver

Internally PD ~150K
Write:0xB6 Read:0xB7

ADDR1	ADD0	Address (R/W)
L	L	0x96/0x97
L	H	0x98/0x99
H	L	0xB6/0xB7
H	H	0xB8/0xB9



SYNC MASTER=YONAS J30 SYNC DATE=11/08/2011

PAGE TITLE: SATA/IR/SIL Connectors

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DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

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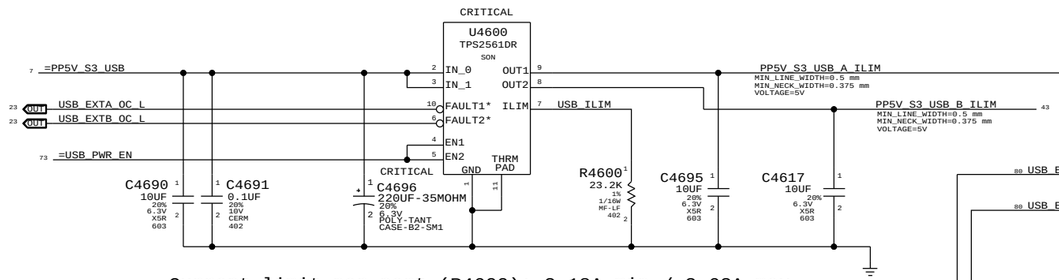
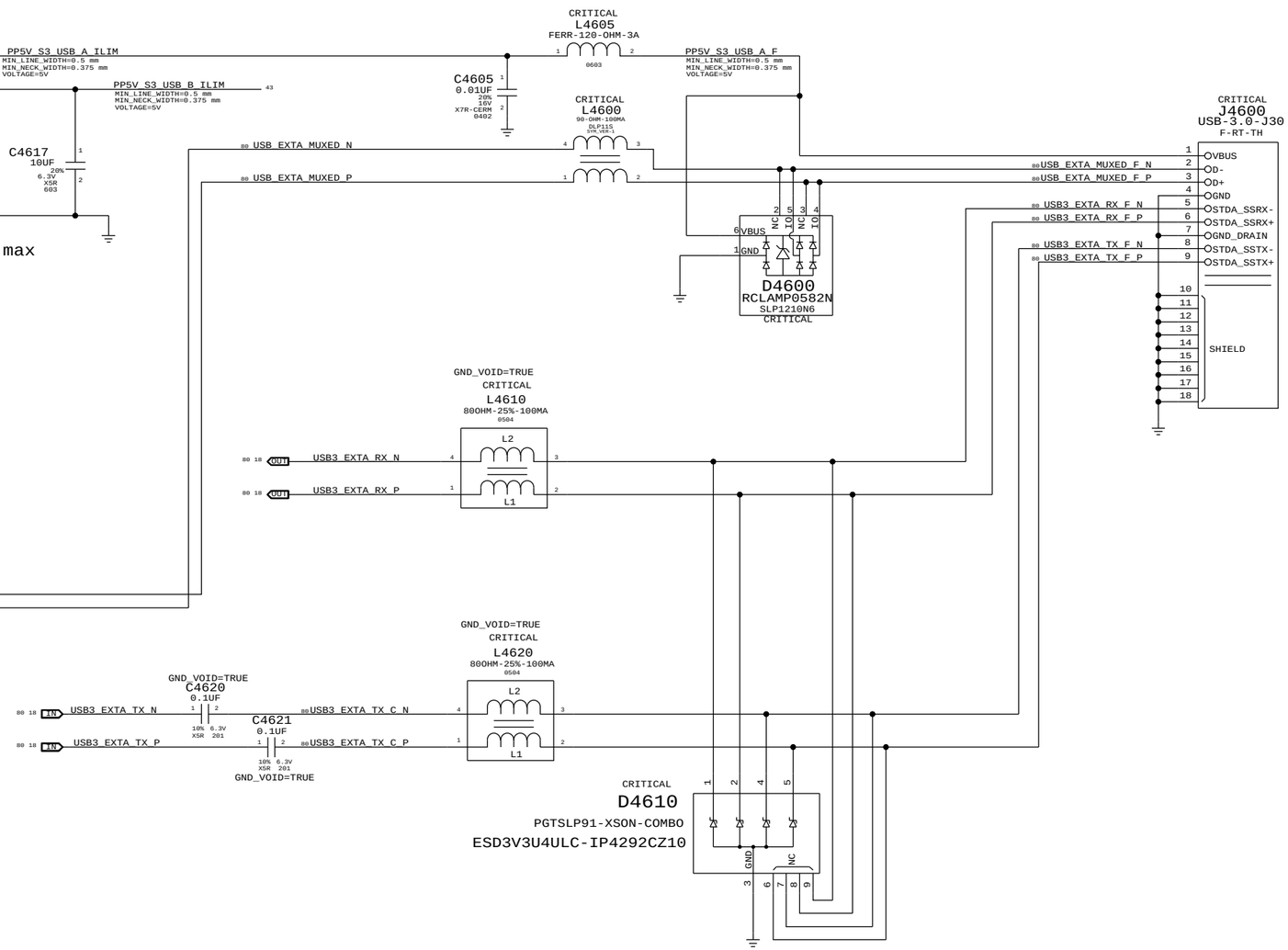
USB Port Power Switch

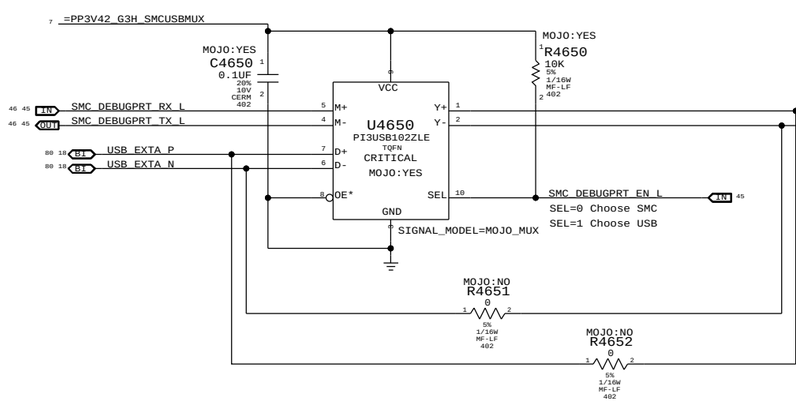


Current limit per port (R4600): 2.18A min / 2.63A max

USB Port A (Front Port)



Mojo SMC Debug Mux



SYNC_MASTER=J31_MLB	SYNC_DATE=07/08/2011
PAGE TITLE: External A USB3 Connector	
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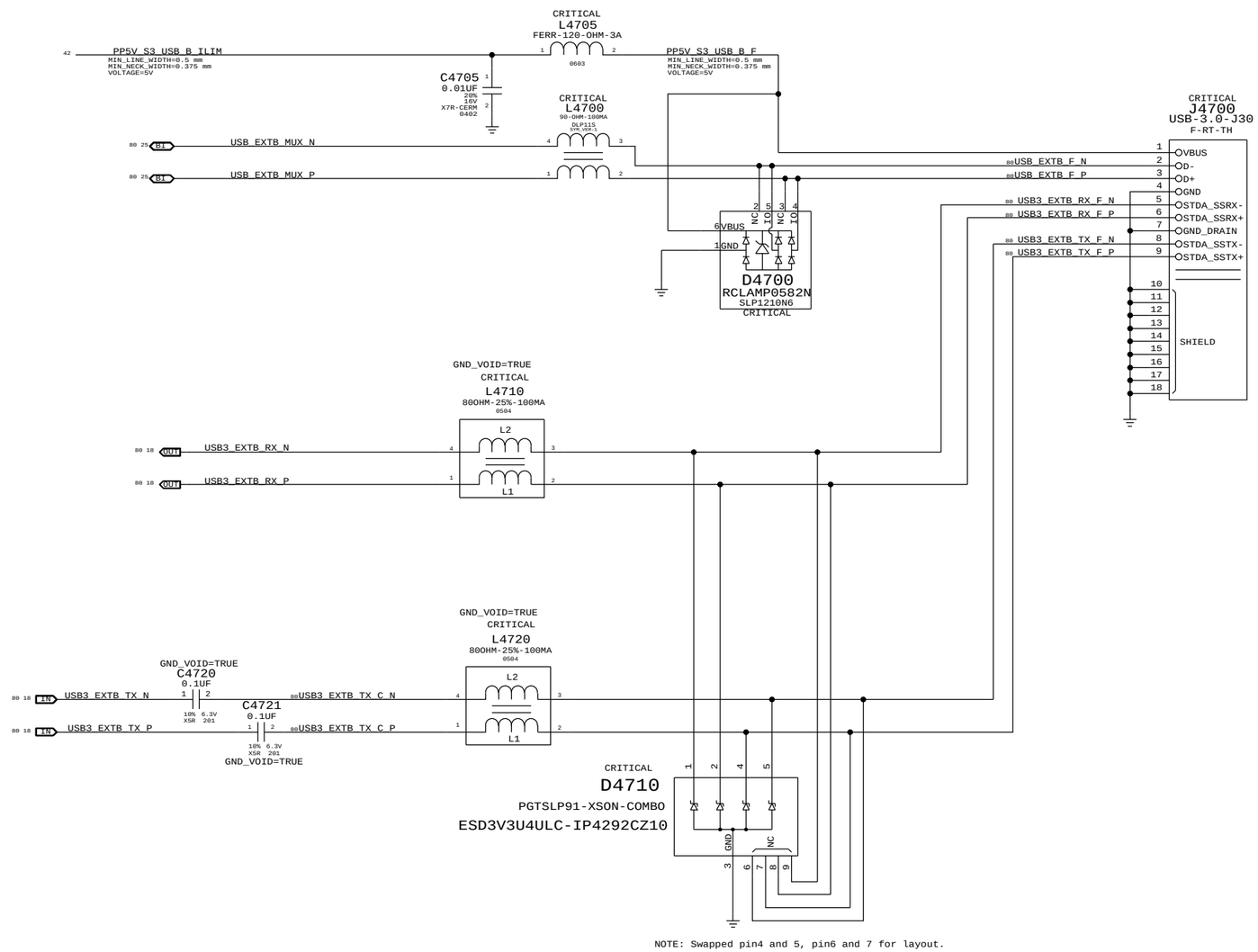
USB Port B (Back Port)



NOTE: Swapped pin4 and 5, pin6 and 7 for layout.

SYNC MASTER=J31_MLB SYNC DATE=07/08/2013

PAGE TITLE

External B USB3 Connector

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

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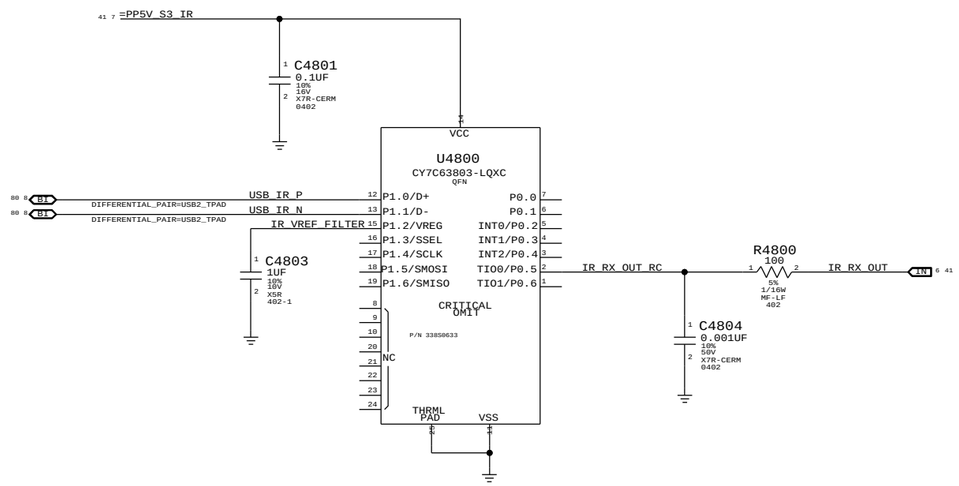
IR SUPPORT



SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE
Front Flex Support

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

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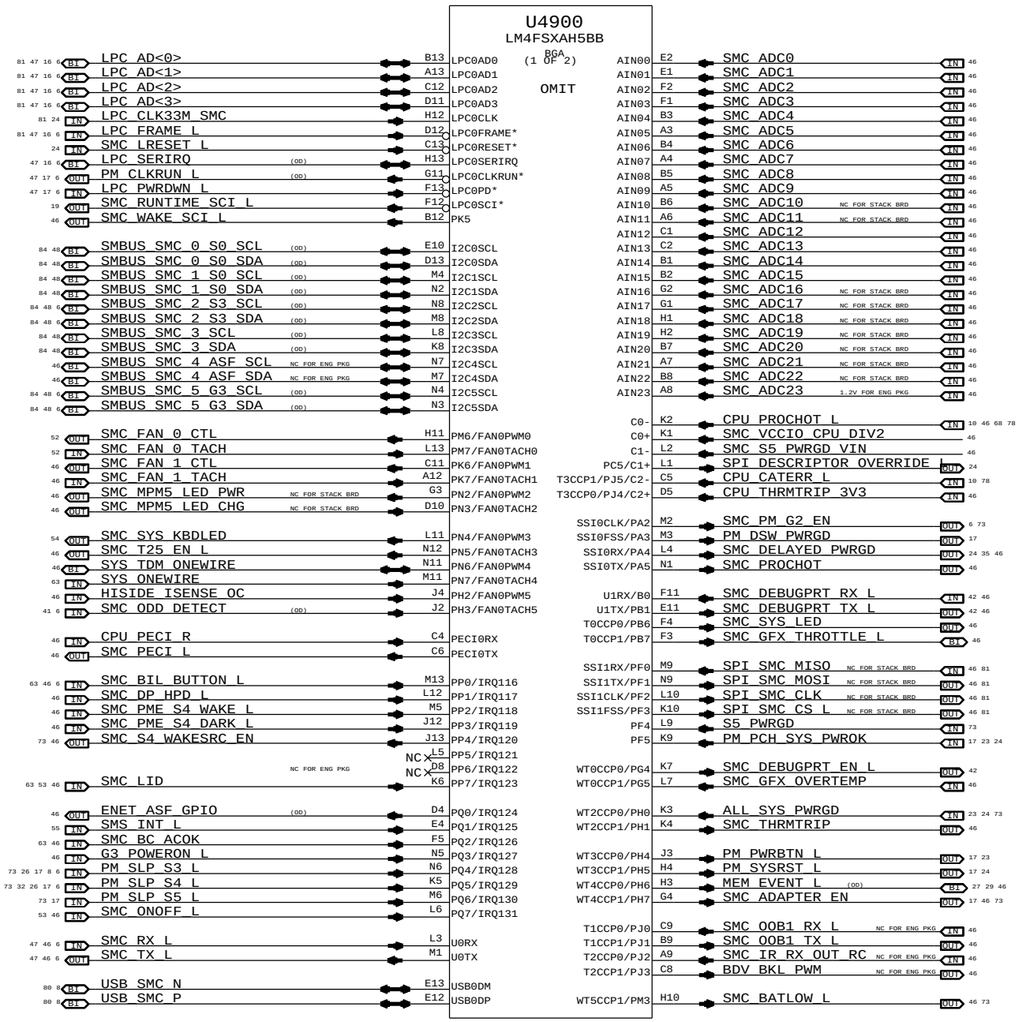

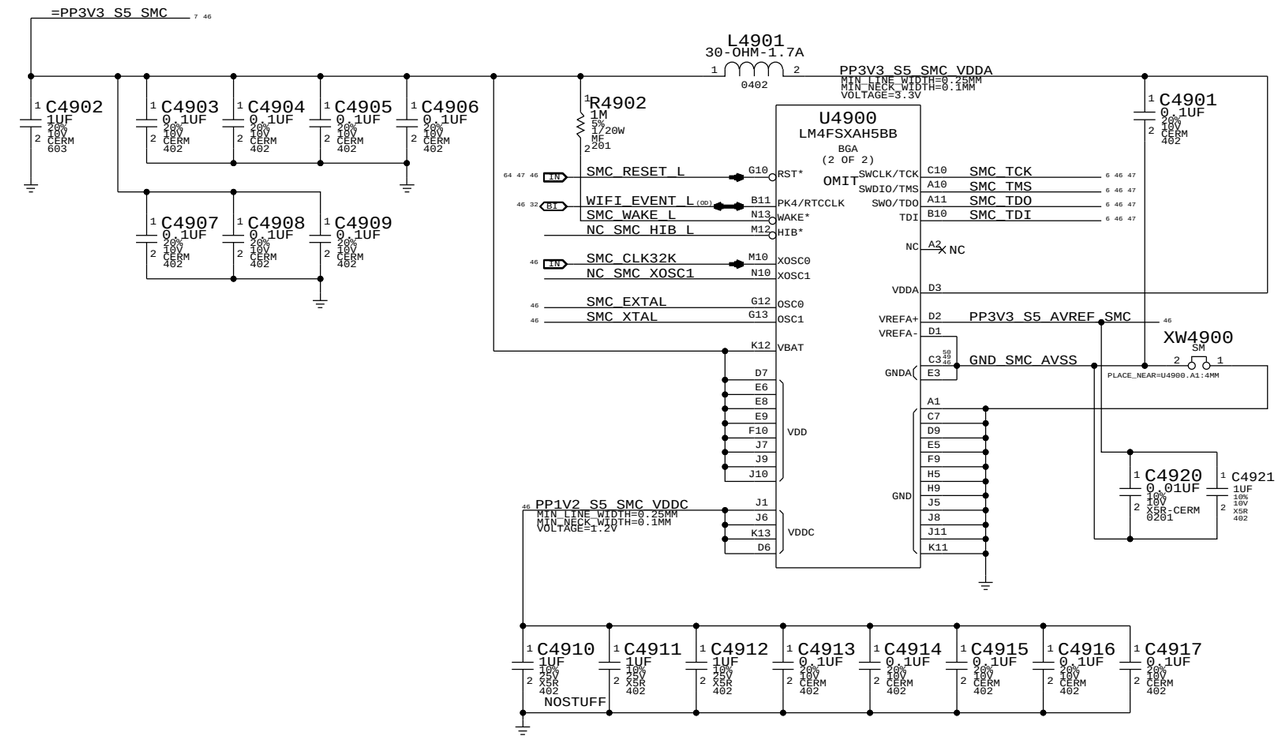

NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SYNC_MASTER=YONAS_J30 SYNC_DATE=12/21/2011

PAGE TITLE
SMC

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D
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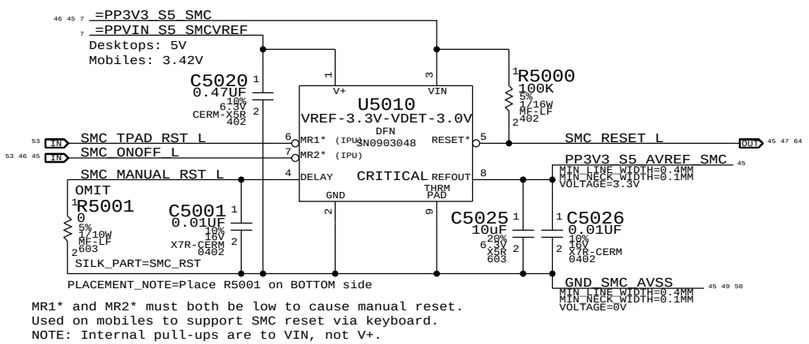
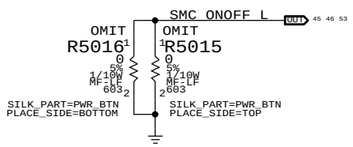
SMC Reset "Button", Supervisor & AVREF Supply



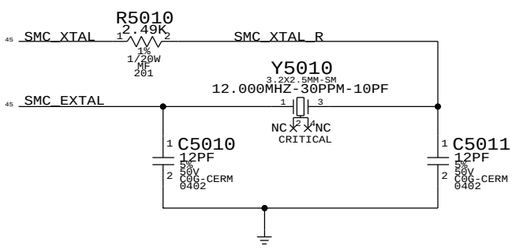
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.
NOTE: Internal pull-ups are to VIN, not V+.

Debug Power "Buttons"



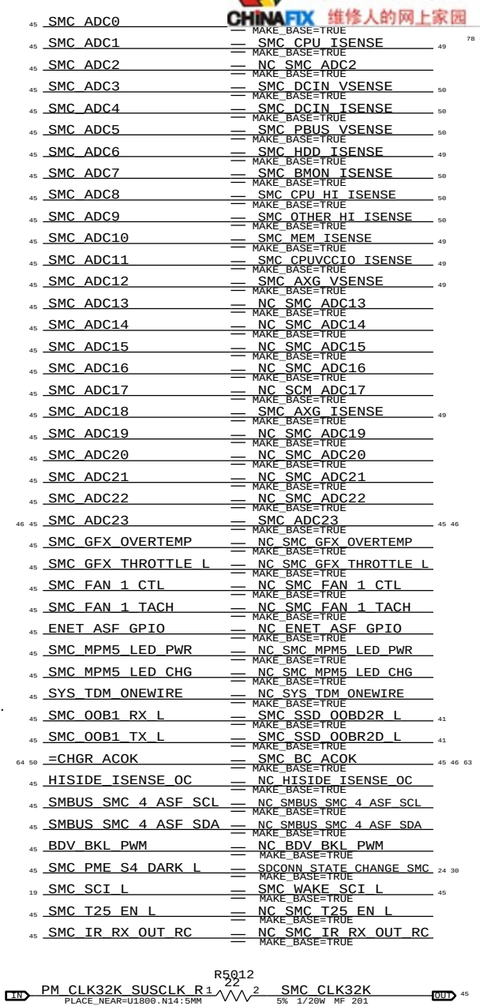
SMC Crystal Circuit

SMC USB Clock require these crystal values:5,6,8,10,12,16,18,20,24,25 MHz

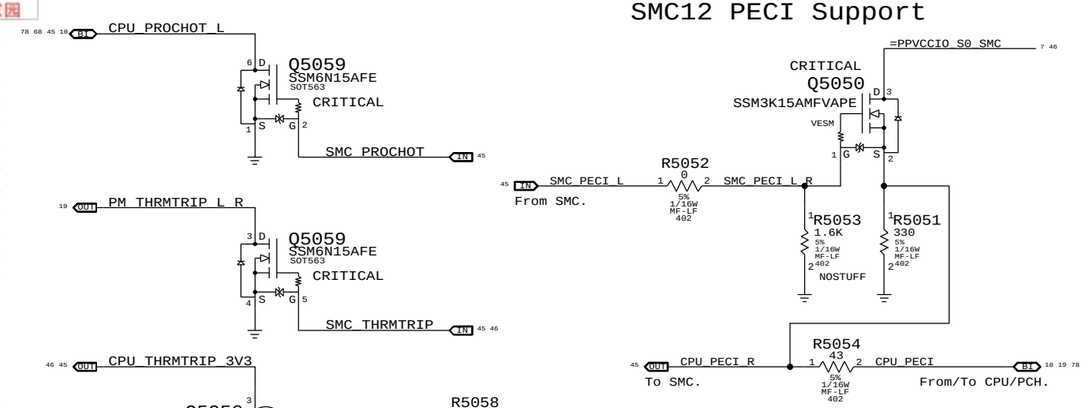


Note:
ADC10 and ADC11 are shared with comparators on Stack Board.

Note:
Pull-up for SMC_PME_S4_DARK_L are in page33 (R3315).

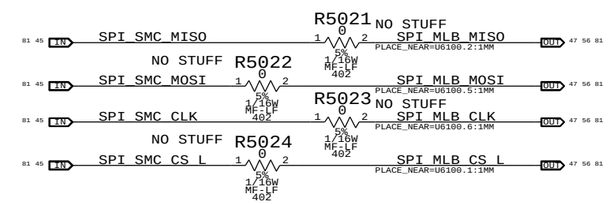


SMC12 PECI Support



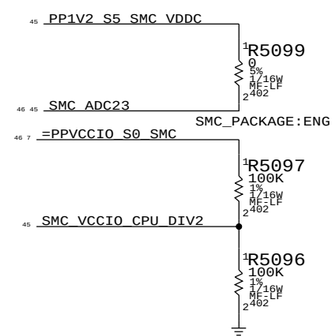
SMC12 SPI Support

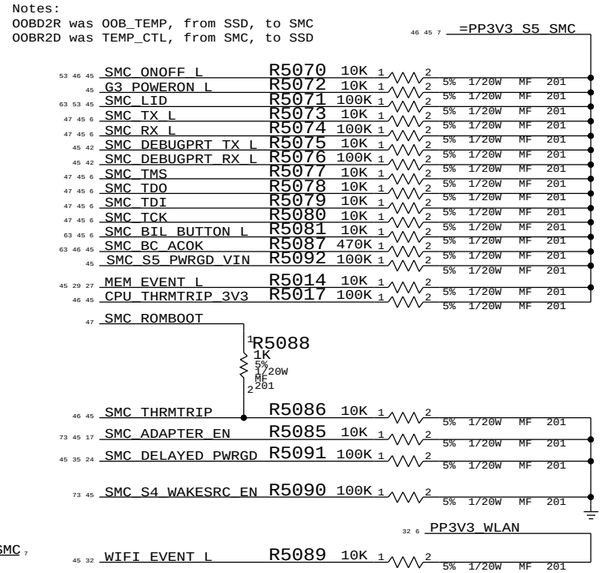
Series resistors are no stuffed until the topology of 2 SPI Masters are verified.



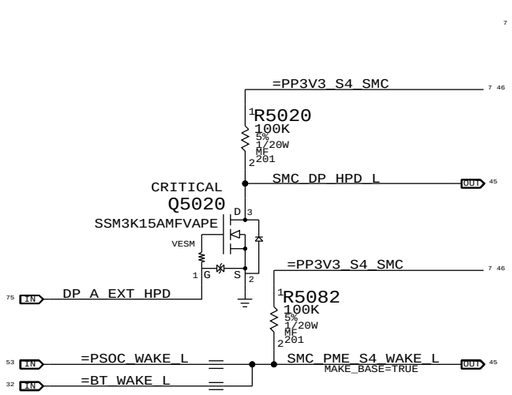
Notes:
OOBD2R was OOB_TEMP, from SSD, to SMC
OOBR2D was TEMP_CTL, from SMC, to SSD

SCM12 Eng Pkg Support

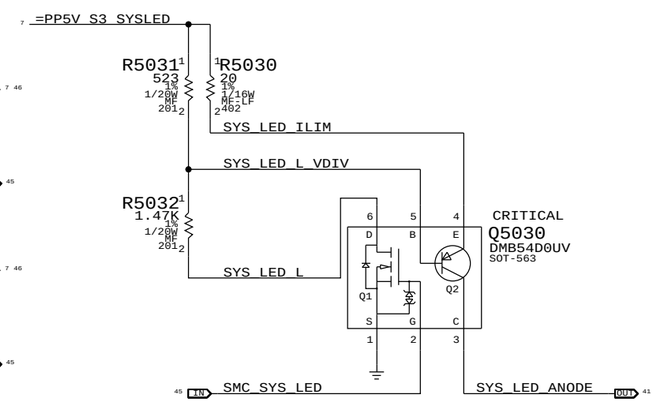




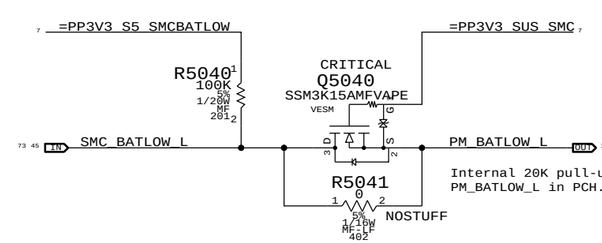
S4 HPD SMC Wake Source



System (Sleep) LED Circuit



BATLOW# Isolation



Internal 20K pull-up on PM_BATLOW_L in PCH.

SYNC_MASTER=YONAS_J30 SYNC_DATE=01/02/2012

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SMC Support

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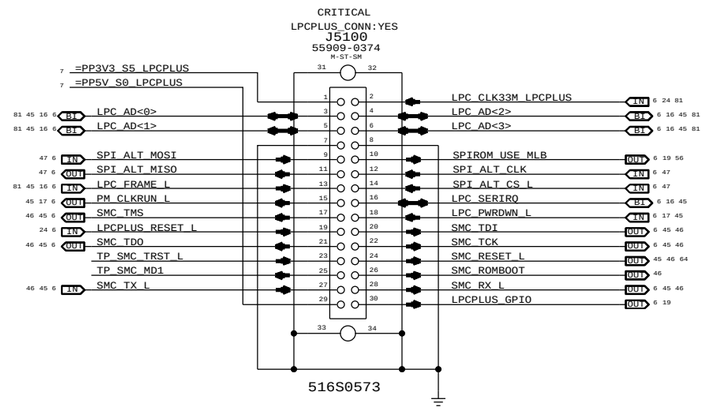
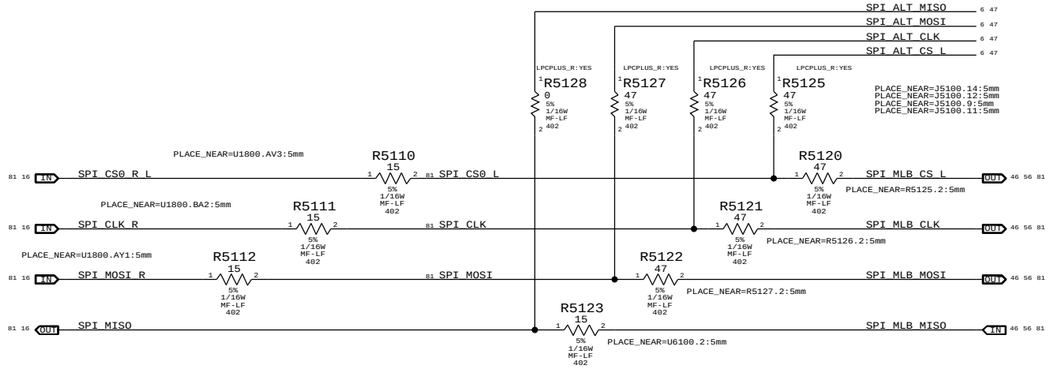
LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=J31_MLB SYNC DATE=06/15/2013

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LPC+SPI Debug Connector

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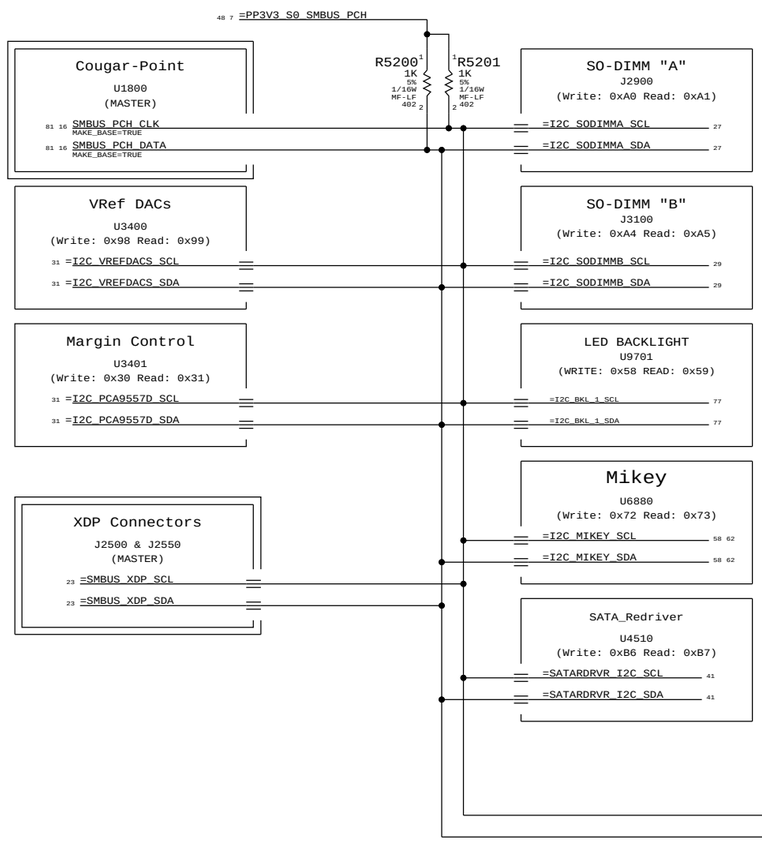
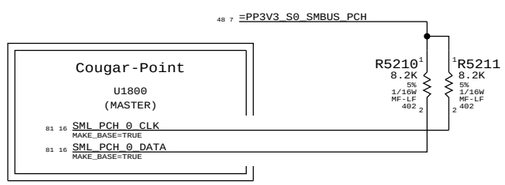
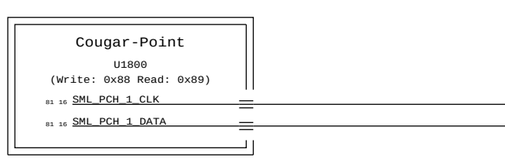
PCH SMBus "0" Connections



PCH "SMLink 0" Connections

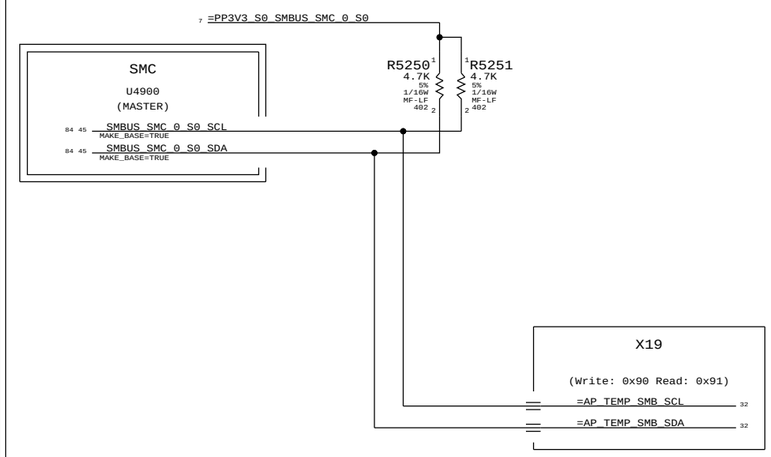


PCH "SMLink 1" Connections



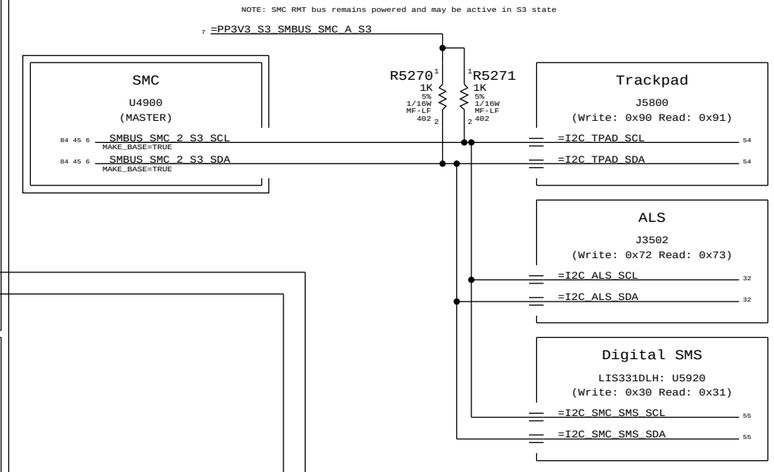
SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

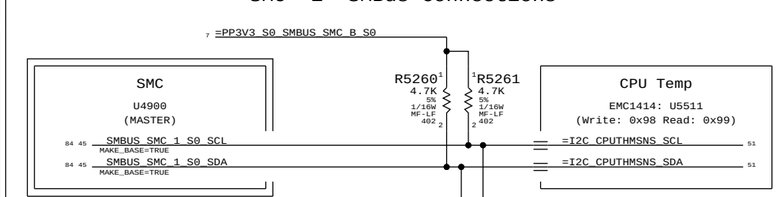


SMC "2" SMBus Connections

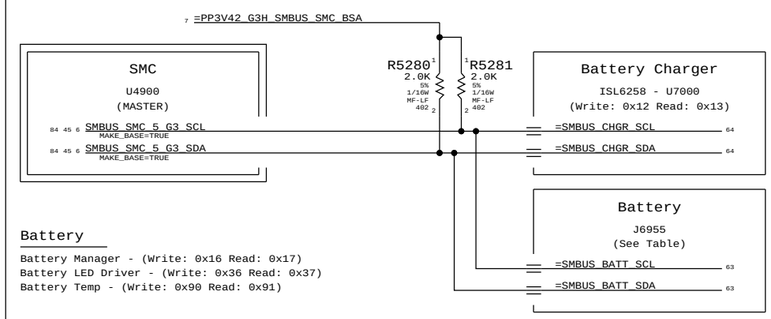
NOTE: SMC RMT bus remains powered and may be active in S3 state



SMC "1" SMBus Connections



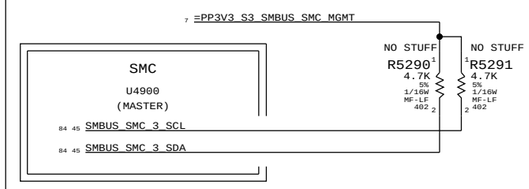
SMC "5" SMBus Connections



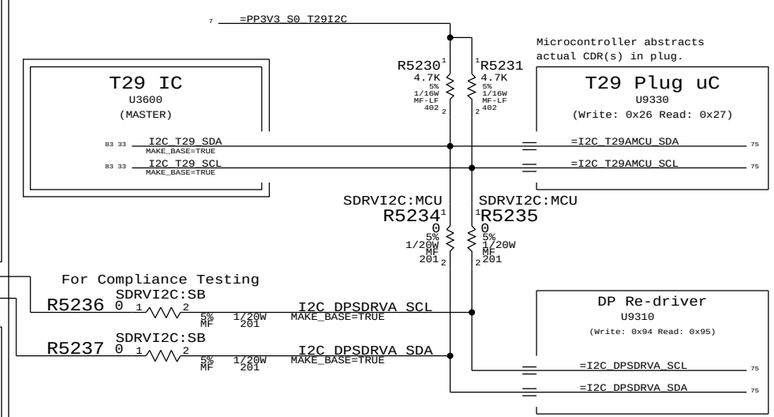
Battery

Battery Manager - (Write: 0x16 Read: 0x17)
Battery LED Driver - (Write: 0x36 Read: 0x37)
Battery Temp - (Write: 0x90 Read: 0x91)

SMC "3" SMBus Connections



T29 I2C Connections



SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2013

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SMBus Connections

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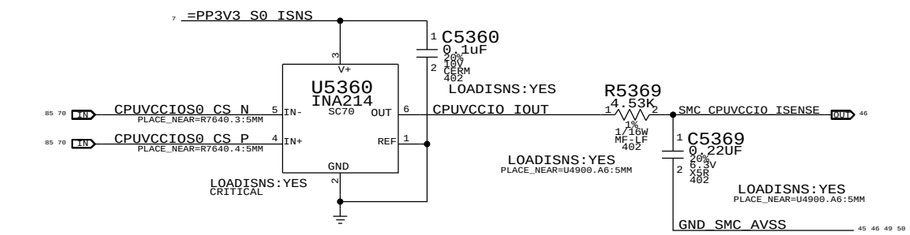
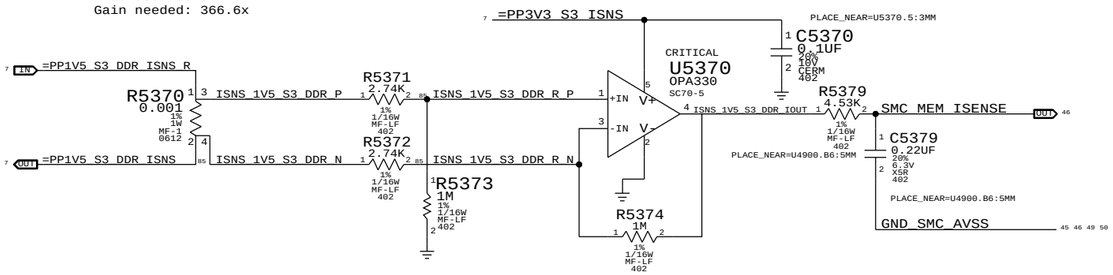
CPU VCCIO 1.05V Load Side Current Sense (IC1C)

Gain: 100x, EDP: 20.1 A
Rsense: 0.001 (R7640)
V across Rsense: 20.1 mV
Gain needed: 164.2x



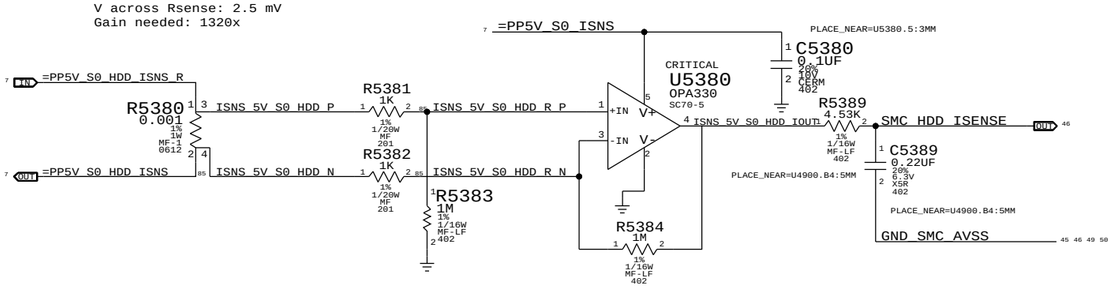
DDR 1.5V S3 (Memory) Current Sense (IM0C)

Gain: 364.9x, EDP: 9 A
Rsense: 0.001 (R5370)
V across Rsense: 9 mV
Gain needed: 366.6x

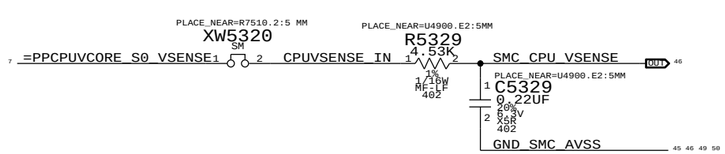


HDD Current Sense (IHDC)

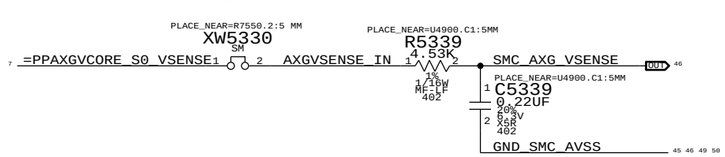
Gain: 1000x, EDP: 2.5 A (12.5 W)
Rsense: 0.001 (R5380)
V across Rsense: 2.5 mV
Gain needed: 1320x



CPU VC0C

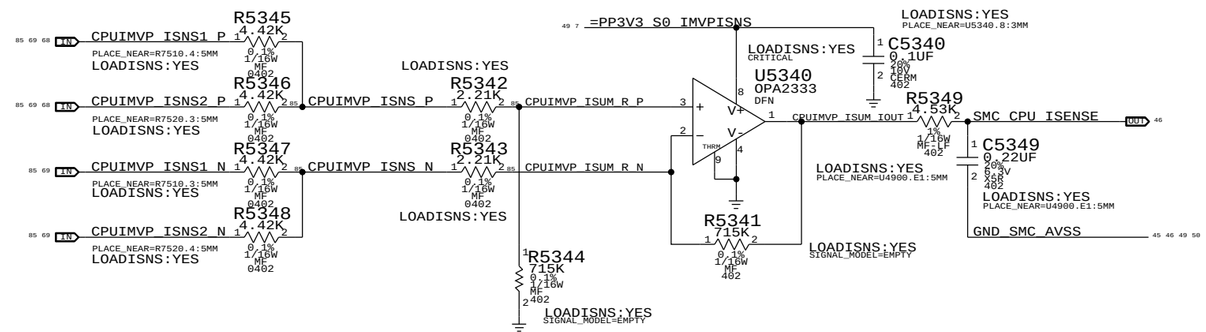


AXG Core Voltage Sense (VN0C)



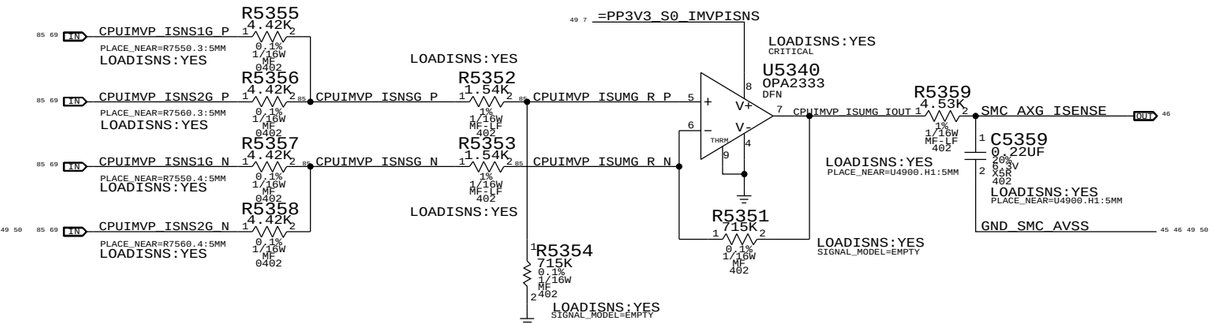
CPU Core Load Side Current Sense (IC0C)

Gain: 161.5x, EDP: 53 A
Rsense: 2x of 0.00075 (R7510, R7520), Rsum: 0.000375
V across Rsense: 19.8 mV
Gain needed: 166.1x



AXG Core Load Side Current Sense (IN0C)

Gain: 190.6x, EDP: 46 A
Rsense: 2x of 0.00075 (R7550, R7560), Rsum: 0.000375
V across Rsense: 17.25 mV
Gain needed: 191.3x



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0114	3	RES,MTL FLIM,100K,1/16W,0402,SMD,LF	C5349,C5359,C5369		LOADISNS:NO

SYNC_MASTER=LINDA_J30 SYNC_DATE=09/28/2011

PAGE TITLE: Power Sensors: Load Side

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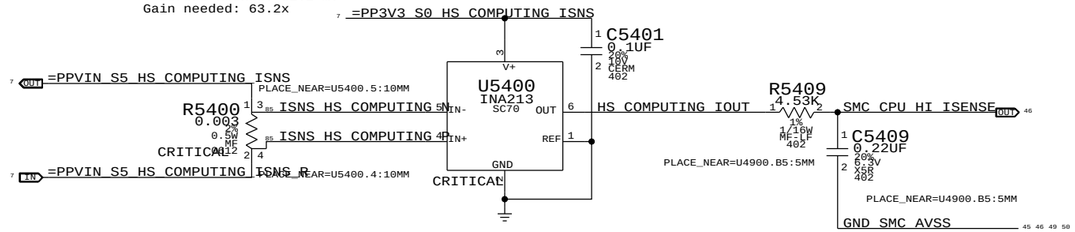
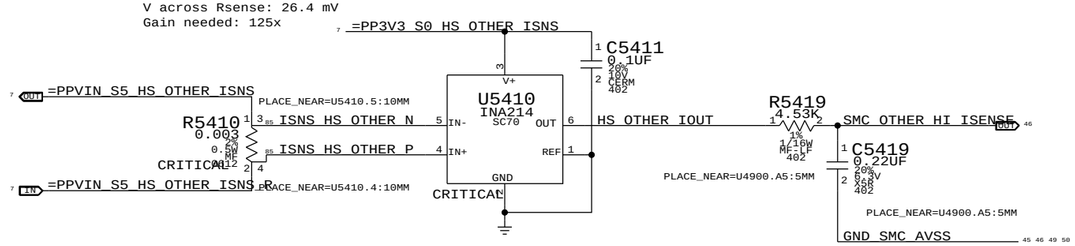
CPU High Side Current Sense (IC0R)

Gain: 50x, EDP: 17.4 A
Rsense: 0.003 (R5400)
V across Rsense: 52.2 mV
Gain needed: 63.2x



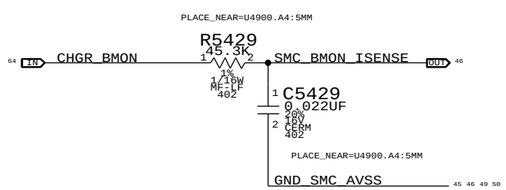
OTHER High Side Current Sense (IO0R)

Gain: 100x, EDP: 8.8 A
Rsense: 0.003 (R5410)
V across Rsense: 26.4 mV
Gain needed: 125x



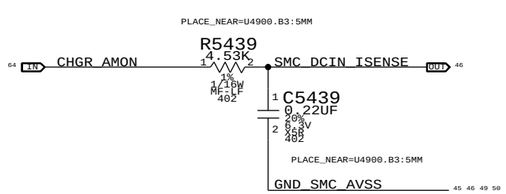
Charger (BMON Production) Current Sense (IPBR)

Charger Gain: 36x
Rsense: 0.010 (R7050)
Max Current Measured: 9.2 A

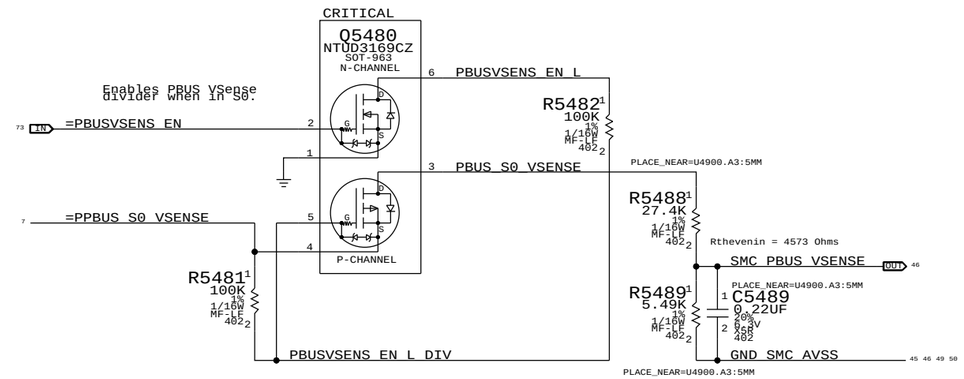


DC-In (AMON) Current Sense (ID0R)

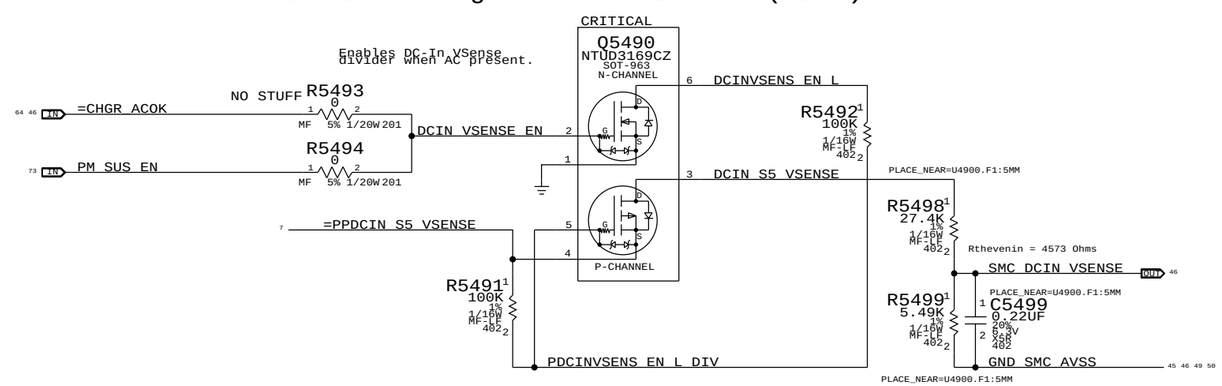
Charger Gain: 20x
Rsense: 0.020 (R7020)
Max Current Measured: 8.3 A



PBUS Voltage Sense & Enable (VP0R)



DC In Voltage Sense & Enable (VD0R)



SYNC_MASTER=YONAS_J30 SYNC_DATE=11/03/2011

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Power Sensors: High Side

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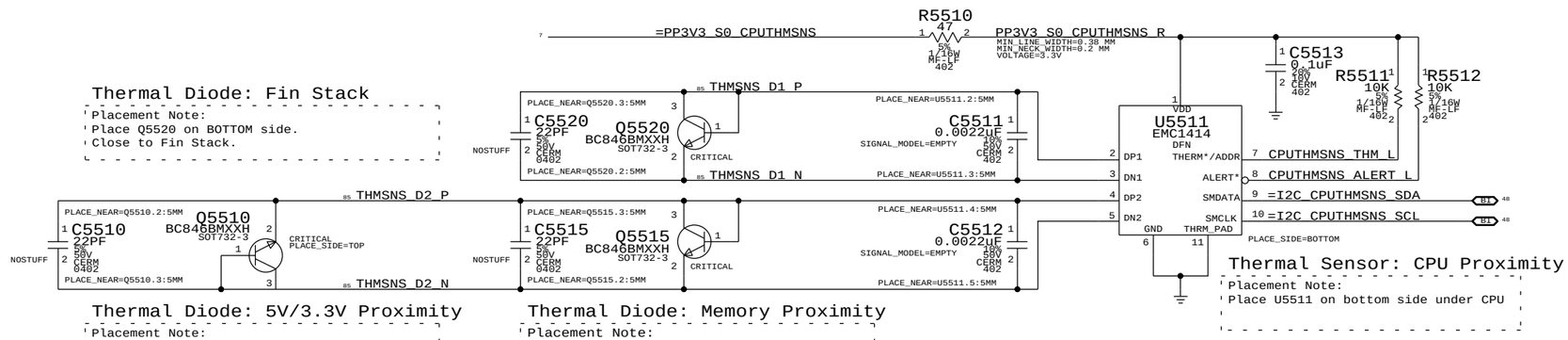
Thermal Sensor:
CPU Proximity, Fin Stack, Memory Proximity, 5V/3.3V Proximity

I2C Write, 0x98, I2C Read: 0x99



Thermal Diode: Fin Stack

Placement Note:
Place Q5520 on BOTTOM side.
Close to Fin Stack.

Thermal Diode: 5V/3.3V Proximity

Placement Note:
Place Q5510 on the TOP side,
Next to 5V and 3.3V power supplies.

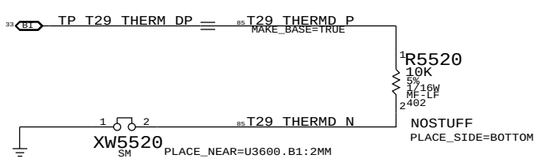
Thermal Diode: Memory Proximity

Placement Note:
Place Q5515 on the EITHER side, on the
right of DIMM connectors.

Thermal Sensor: CPU Proximity

Placement Note:
Place U5511 on bottom side under CPU

Thermal Sensor: T29 Die



Note: Use GND pin B1 on U3600 for N leg.

SYNC_MASTER=YONAS_J30 SYNC_DATE=08/01/2011

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Thermal Sensors

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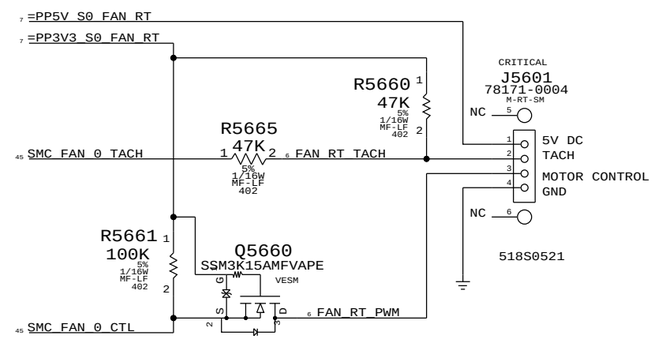

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

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Fan

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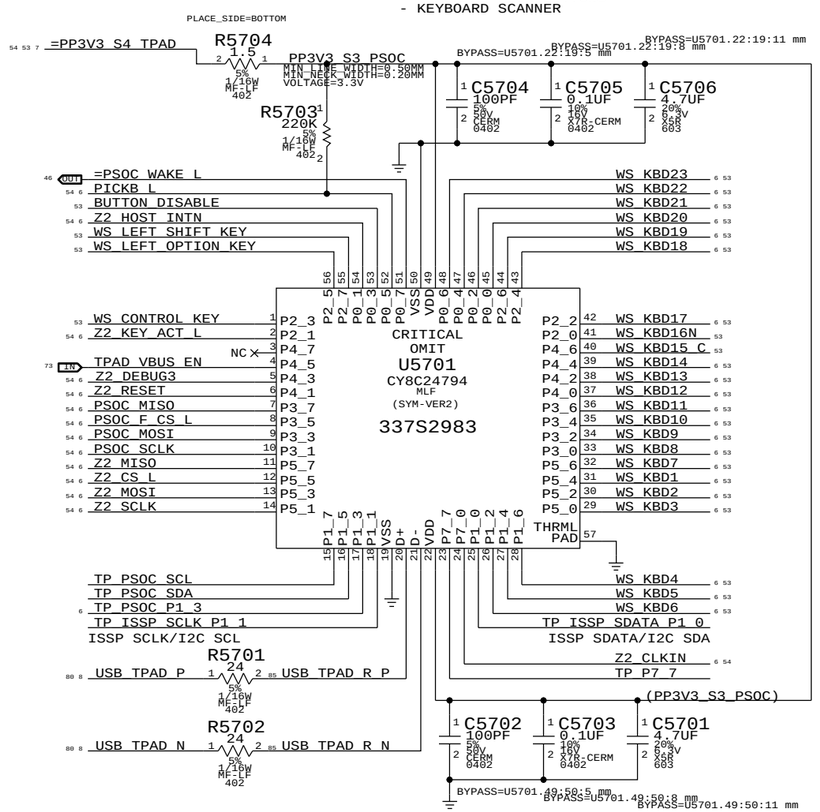
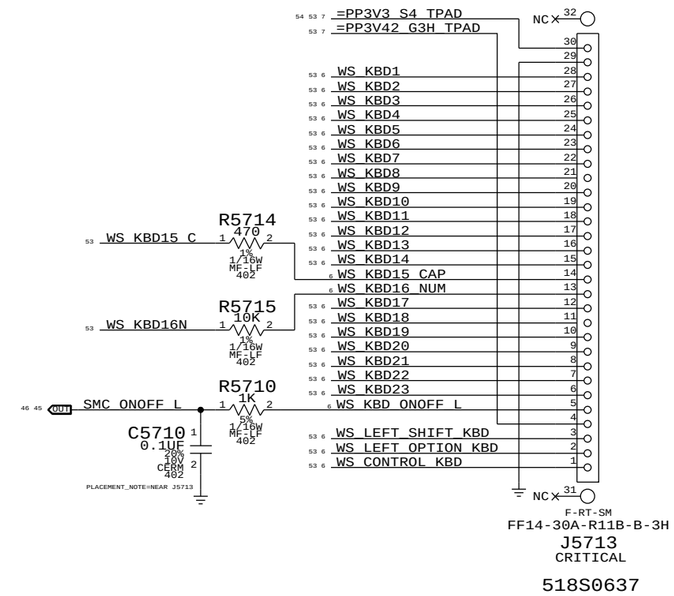
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA 80UA	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD VOUT	60MA (MAX) 60MA (MAX)	10 OHM 0.2 OHM	0.6 V 0.012 V	36E-3 W 0.72E-3 W
PSOC	VDD	8MA (TYP) 14MA (MAX)	1.5 OHM	0.012 V 0.021 V	96E-6 W 294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

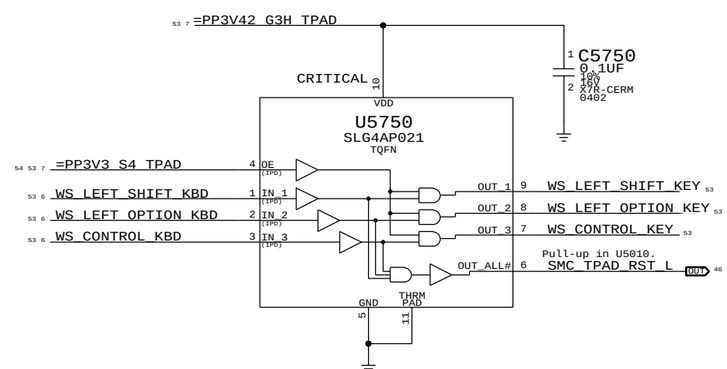
Keyboard Connector



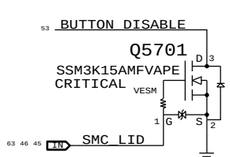
SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.

Keys ANDed with MSP power to isolate when MSP is not powered. No IPD on OE input pin PP3V3_S4 (symbol error).



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC_MASTER=J31_MLB SYNC_DATE=07/01/2011

PAGE TITLE: WELLSPRING 1

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DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

BRANCH:

PAGE: 57 OF 109

SHEET: 53 OF 86

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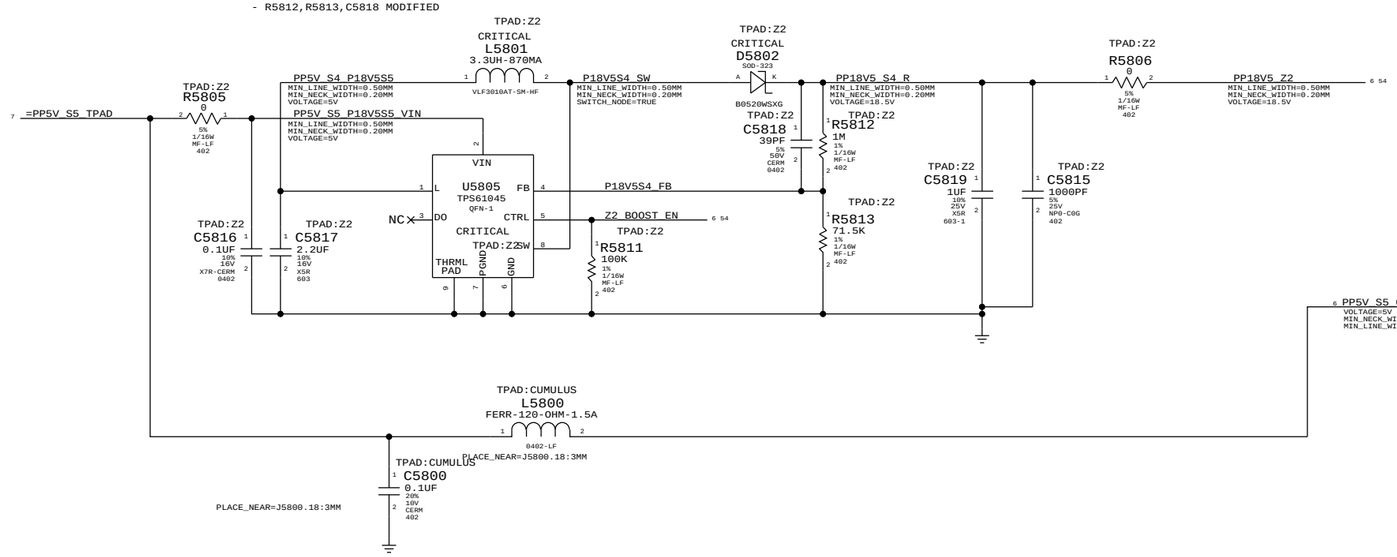
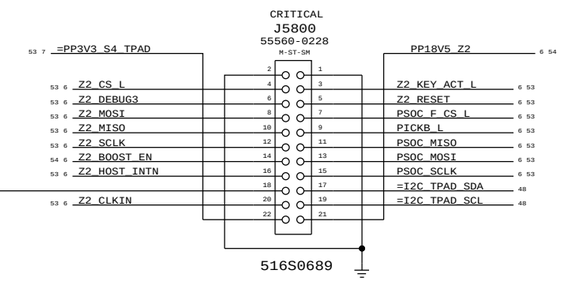
BOOSTER +18.5VDC FOR SENSORS

BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED

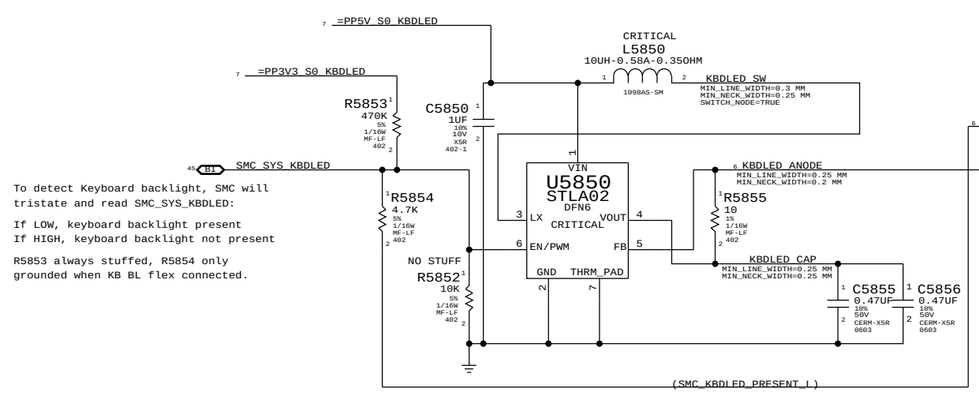


IPD Flex Connector



PIN 21 IS NC ON CUMULUS FLEX
PIN 18 IS NC ON Z2 FLEX

Keyboard Backlight Driver & Detection

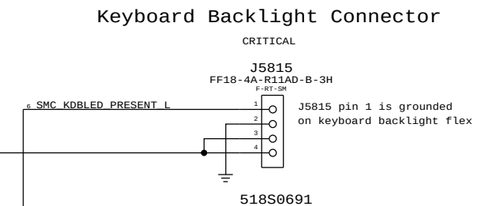


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



J5815 pin 1 is grounded on keyboard backlight flex

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SYNC MASTER=JACK J30 SYNC DATE=09/28/2011
PAGE TITLE
WELLSPRING 2
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DRAWING NUMBER 051-9058 SIZE D
REVISION 6.0.0
BRANCH
PAGE 58 OF 109
SHEET 54 OF 86

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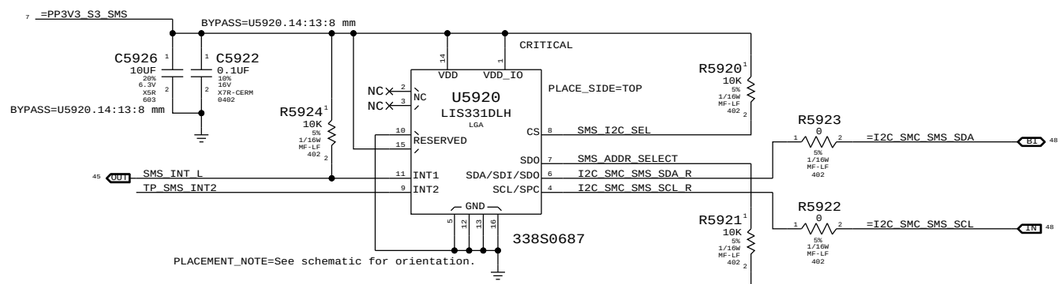
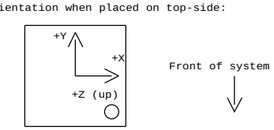


SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

NOTE: SDA and SCL have internal pull-ups to VDD_IO.

Desired orientation when placed on top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE
Digital Accelerometer

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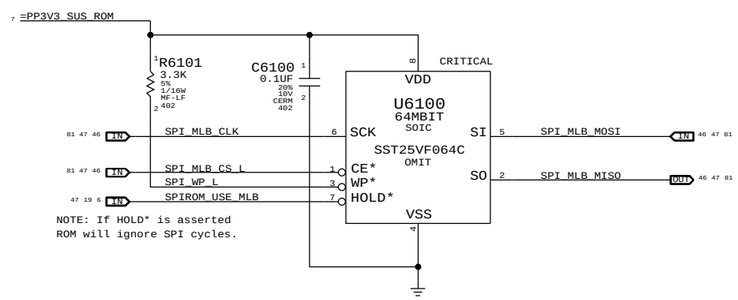

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE

SPI ROM

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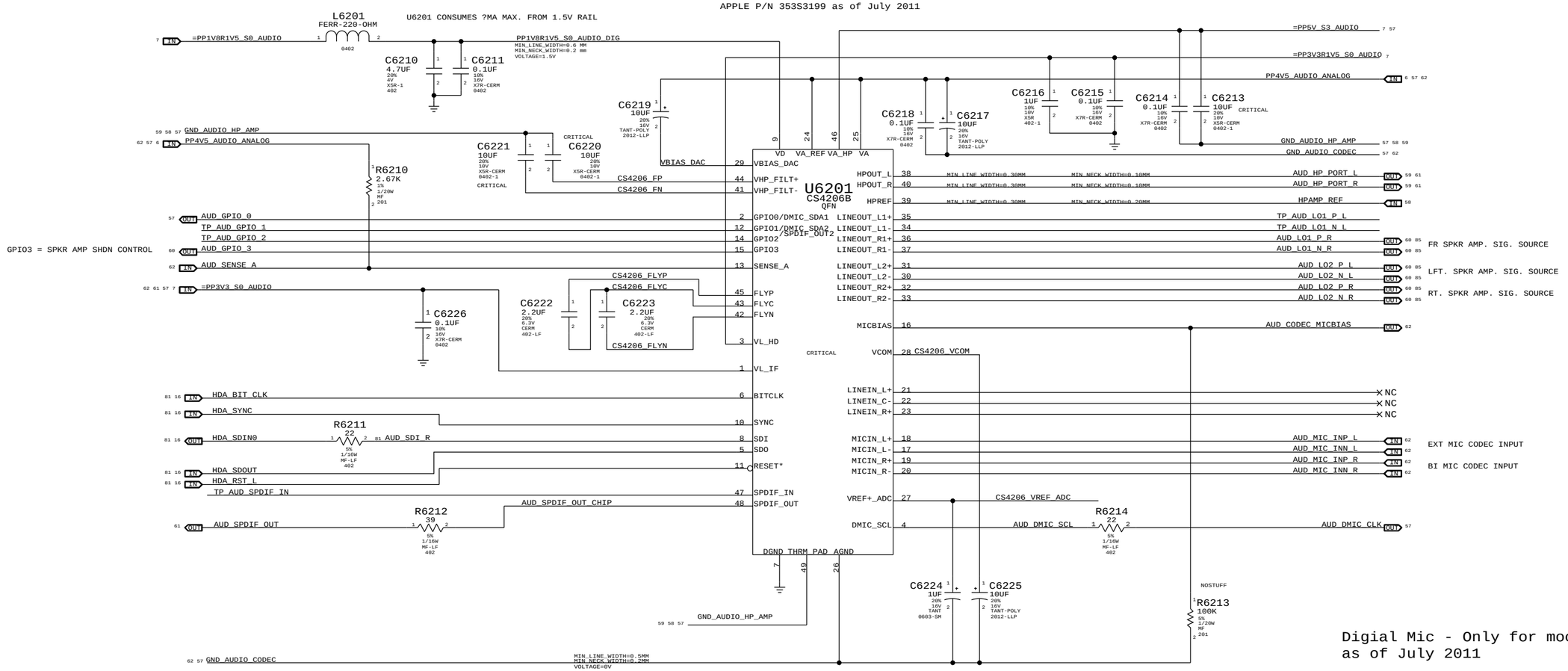
AUDIO CODEC

APPLE P/N 353S3199 as of July 2011



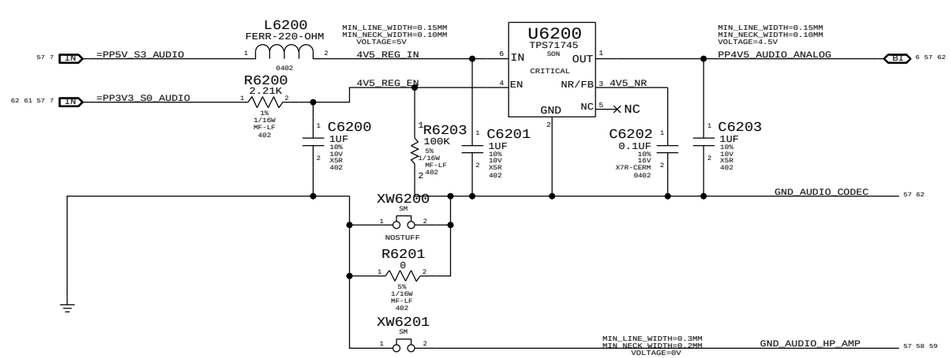
Digial Mic - Only for mock ups
as of July 2011

57 AUD_DMIC_CLK — TP_AUD_DMIC_CLK
MAKE_BASE=TRUE

57 AUD_GPIO_0 — TP_AUD_DMIC_SDATA
MAKE_BASE=TRUE

4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2281 as of July 2011



NOTES ON J30 audio

Codec HPamp used for Lineout/HPout. No external HPamp.
3 Spk amplifiers - 2 tweeters and a sub woofer
No line input capability
SPDIF out
China headset support

SYNC MASTER=KAVITHA_J30 SYNC DATE=07/25/2013

PAGE TITLE
AUDIO: CODEC/REGULATOR

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DRAWING NUMBER 051-9058 SIZE D
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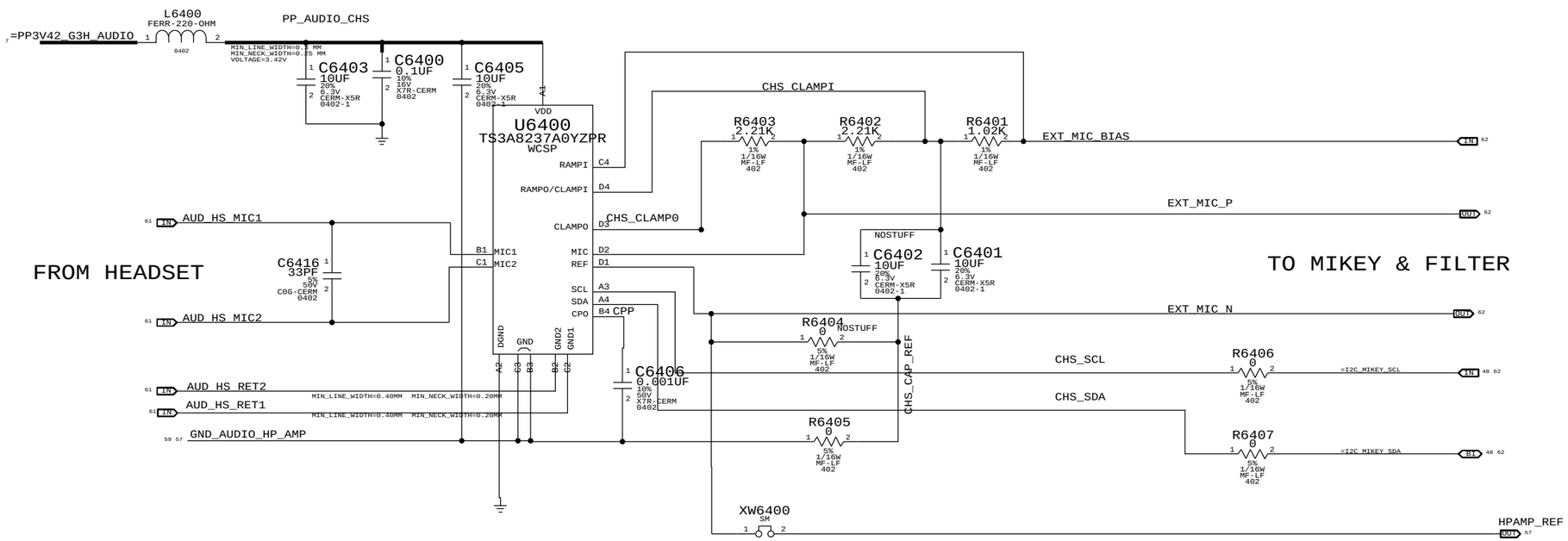
EXTERNAL (HEADSET) MIC INPUT CIRCUITRY APN:353S3066 as of July 2011



I2C ADDRESSES: CHS uses SMBus 0 connections

CHS	U6400	READ	0111	0111	0x77
CHS	U6400	WRITE	0111	0110	0x76

SYNC MASTER=DIRK J30 SYNC DATE=02/16/2012

PAGE TITLE
AUDIO: DETECT/MIC BIAS

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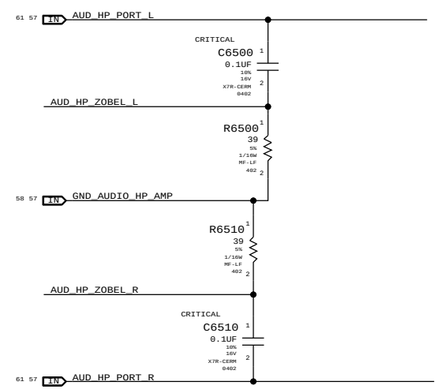
ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



SYNC_MASTER=KAVITHA_J30 SYNC_DATE=07/25/2011

PAGE TITLE
AUDIO: HEADPHONE FILTER

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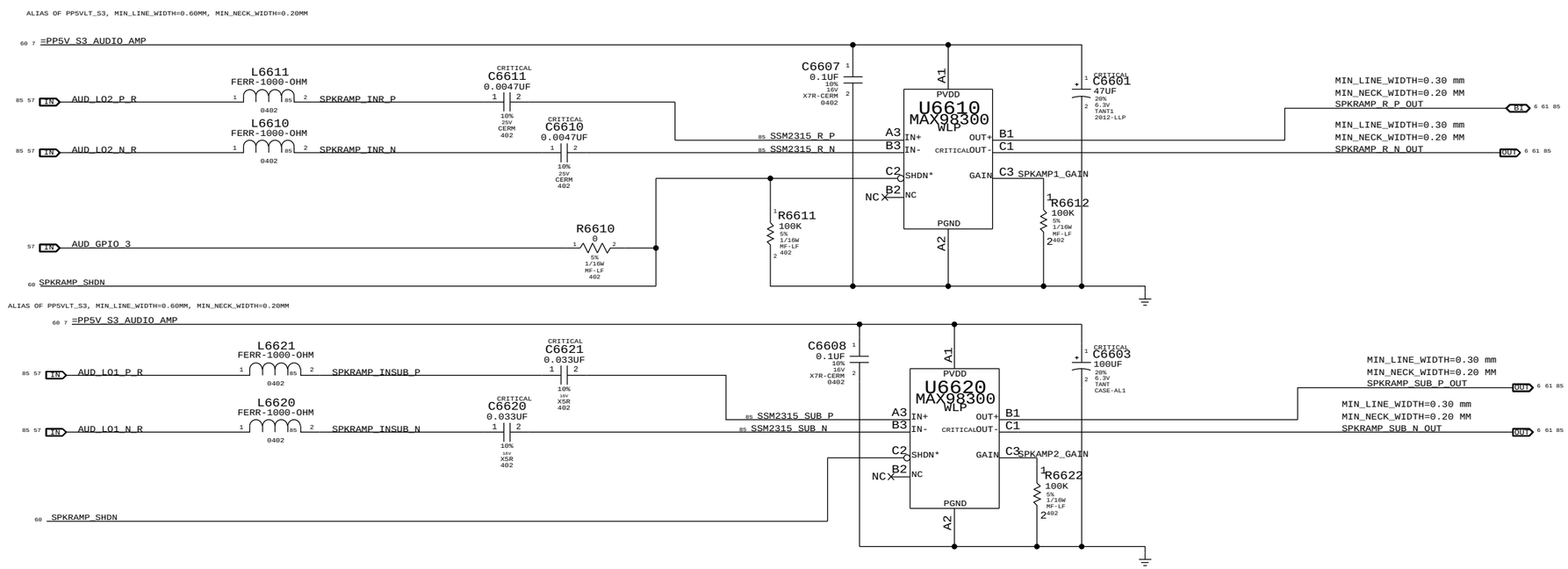
SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2888 as of July 2011

SATELLITE	FC=1.2kHz typical
SUB	FC= 172 HZ typical
GAIN	3DB with Rin=28k typical

Gain Pin	Gain dB
Connect to VDD	12
Connect to VDD through 100k	9
Not connected	6
Connect to GND through 100k	3
Connect to GND	0



SYNC_MASTER=KAVITHA_J30 SYNC_DATE=07/25/2013

PAGE TITLE

AUDI0: SPEAKER AMP

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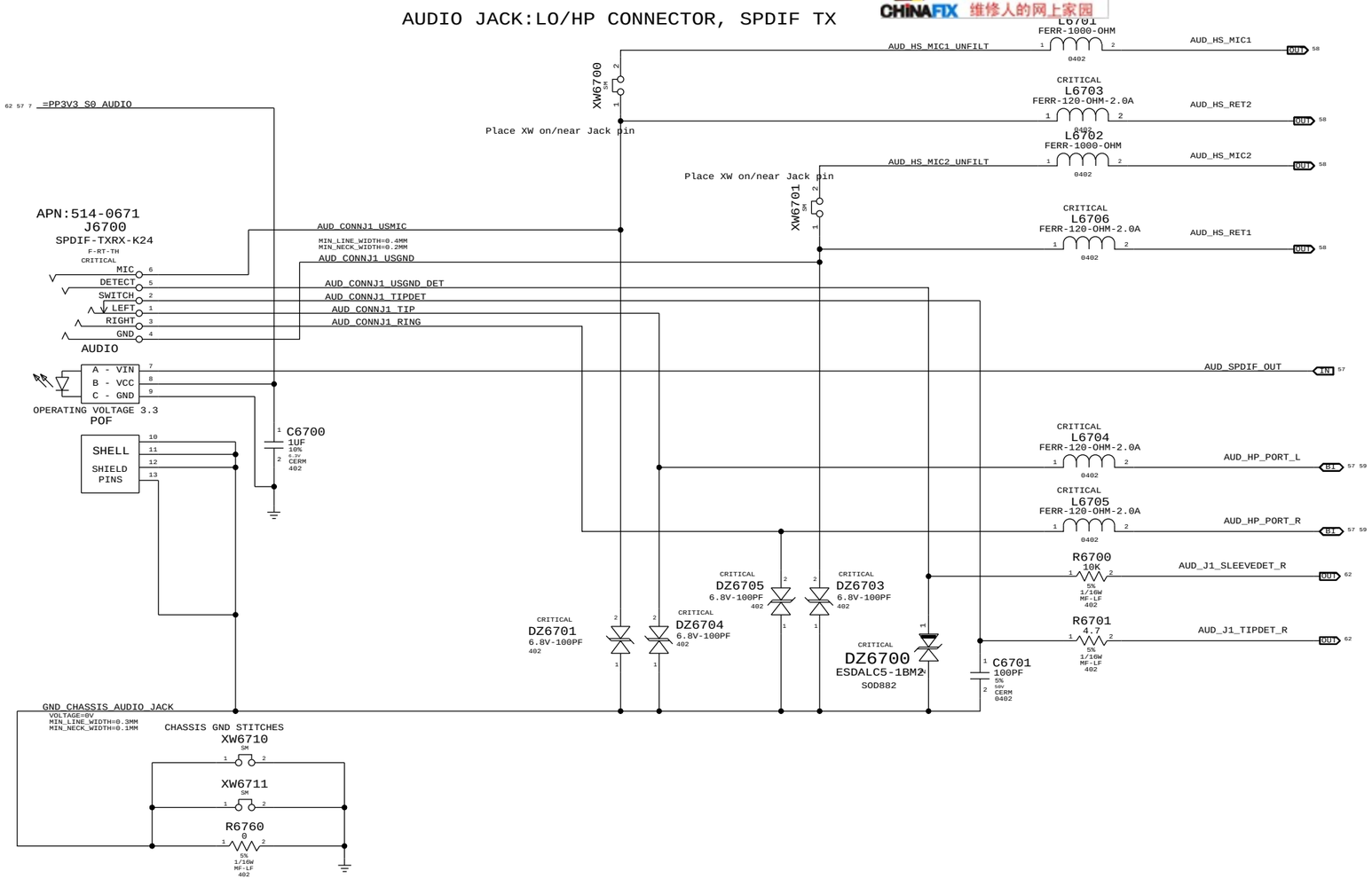
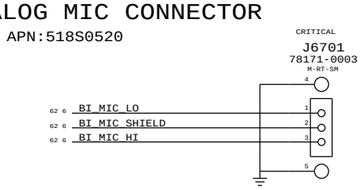
AUDIO JACK:LO/HP CONNECTOR, SPDIF TX



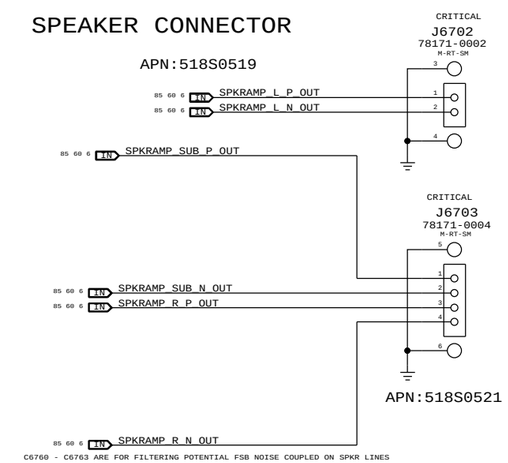
ANALOG MIC CONNECTOR

APN:518S0520



SPEAKER CONNECTOR

APN:518S0519



C6760 - C6763 ARE FOR FILTERING POTENTIAL FSB NOISE COUPLED ON SPKR LINES

SYNC_MASTER=DIRK_J30 SYNC_DATE=11/10/2011

PAGE TITLE

AUDIO: JACK

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CODEC OUTPUT SIGNAL PATHS

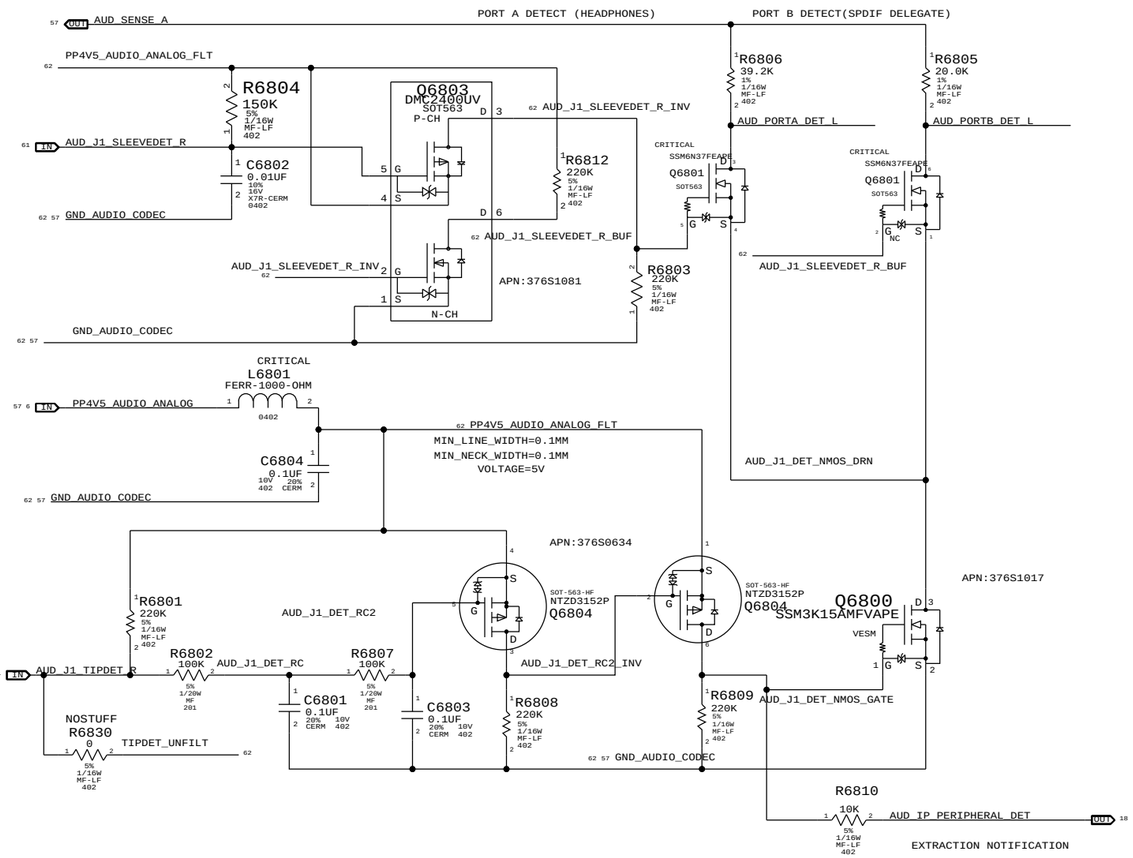
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	N/A	0X09 (A)
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

CODEC INPUT SIGNAL PATHS

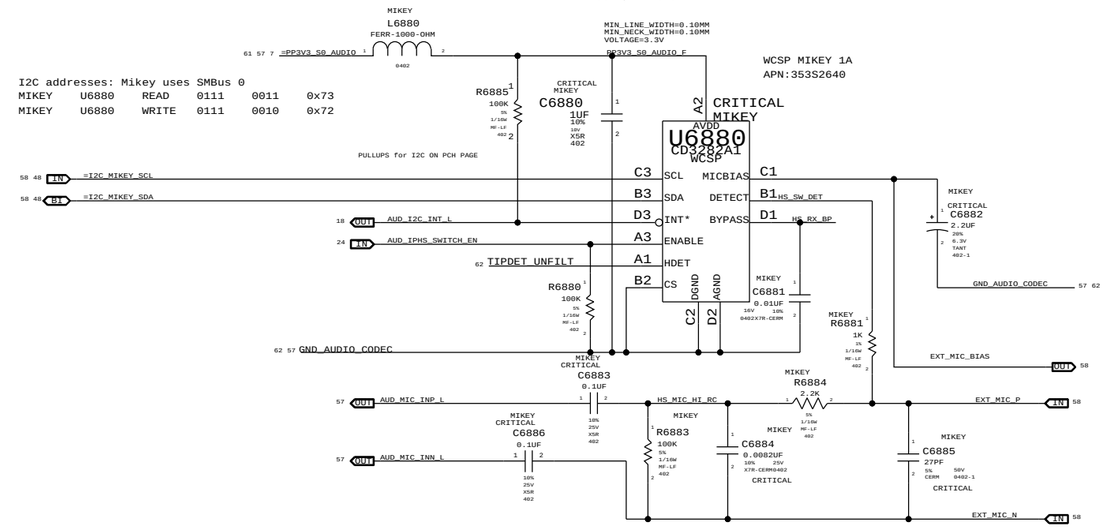
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

SOUTHBRIDGE RESOURCES

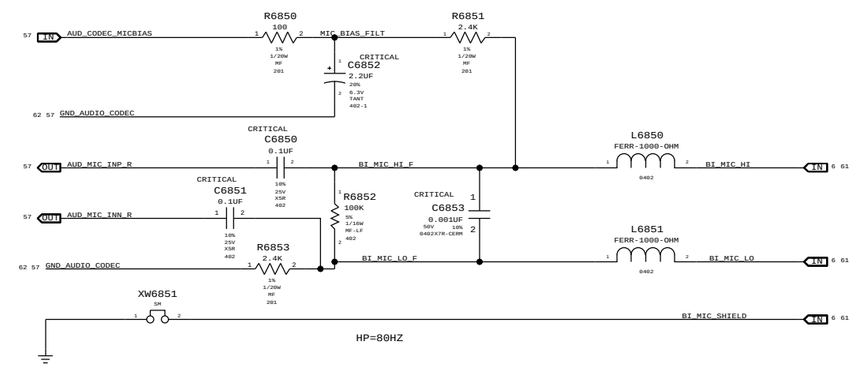
FUNCTION	SYSTEM GPIO	SYSTEM INTERRUPT
AUD_IPHS_SWITCH_EN	PANTHER_POINT GPIO16	N/A
AUD_I2C_INT_L	N/A	PANTHER_POINT GPIO5/PIRQH
AUD_IP_PERIPHERAL_DET	N/A	PANTHER_POINT GPIO3/PIRQH



PORT B LEFT(HEADSET MIC)
HP=80HZ, LP=8.82KHZ



PORT B RIGHT(BUILT-IN MIC)



SYNC MASTER=DIRK_J30 SYNC DATE=02/20/2012

PAGE TITLE
AUDIO:Jack Translators

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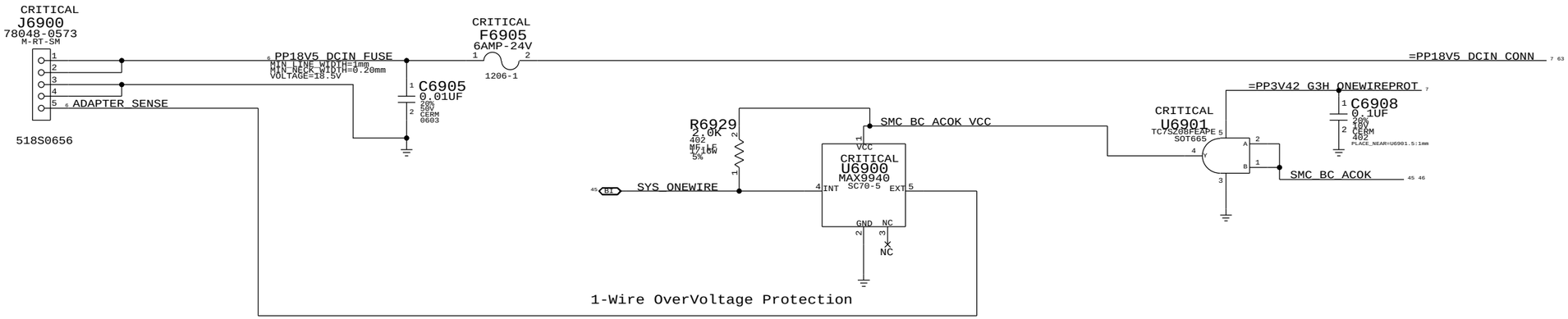
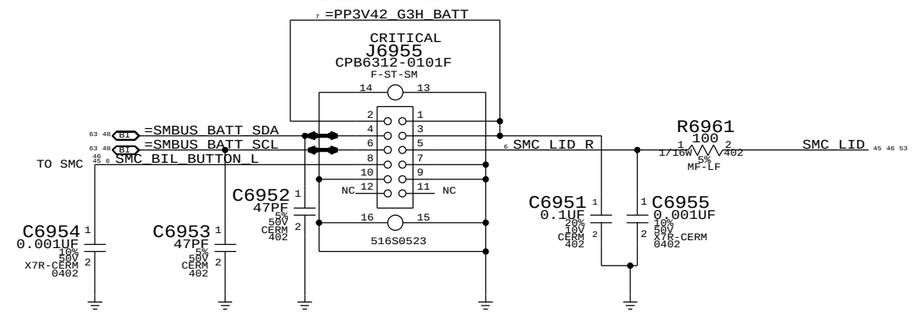
MagSafe DC Power Jack

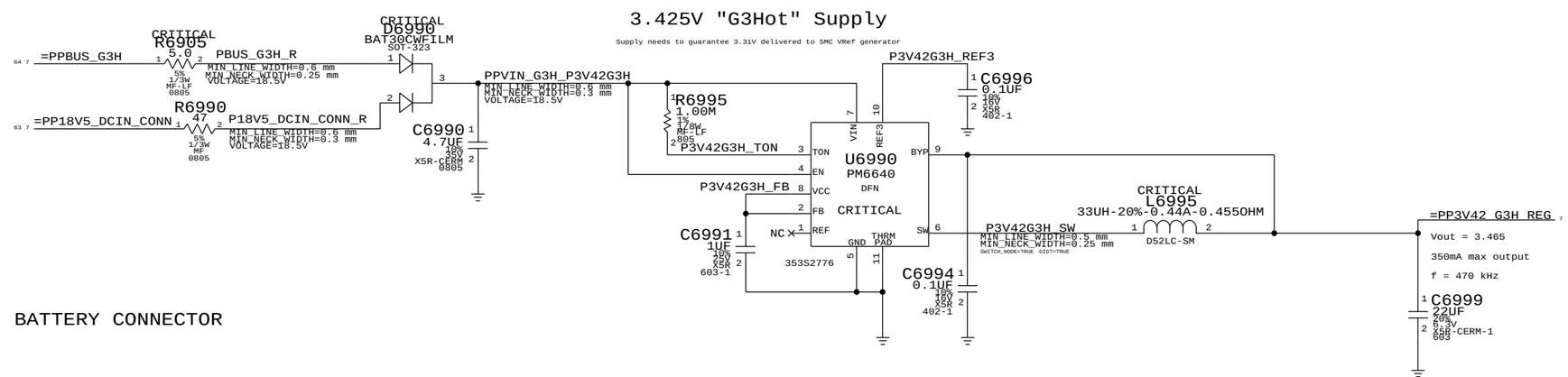


BIL CONNECTOR

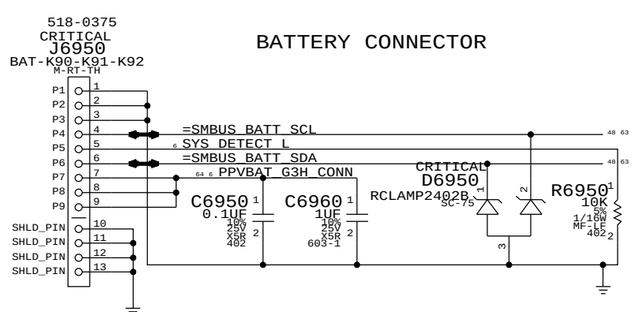


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC_MASTER=JACK_J30	SYNC_DATE=07/29/2011
PAGE TITLE: DC-In & Battery Connectors	
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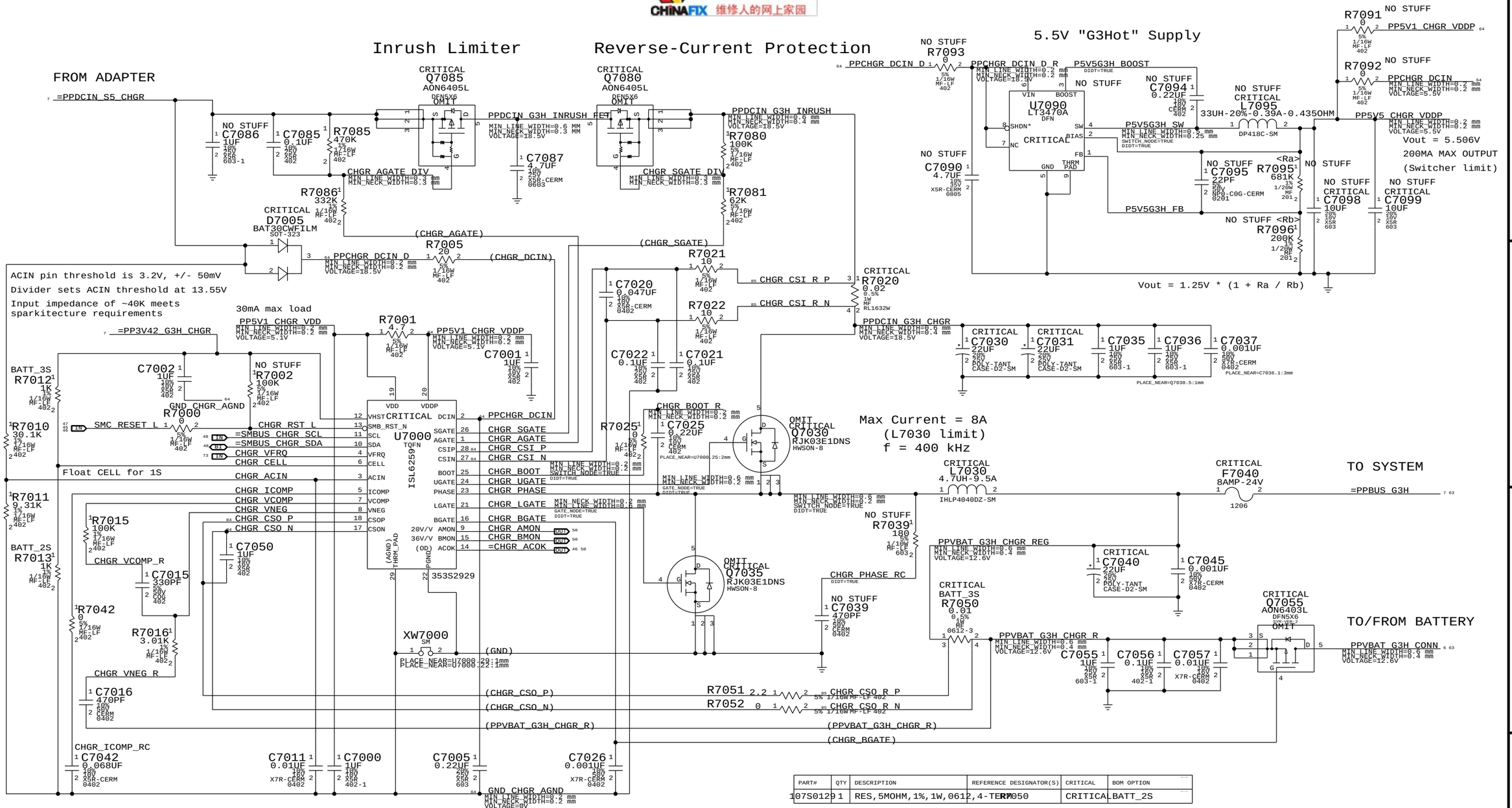

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0129	1	RES,5MOHM,1%,1W,0612,4-TERM	R7050	CRITICAL	BATT_2S

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0927	2	FDMC3020DC	Q7030,Q7035	CRITICAL	CHARGER_POWER_FET:FAIR
376S0966	2	RJK03E1DNS	Q7030,Q7035	CRITICAL	CHARGER_POWER_FET:REN

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0761	1	SI7137DP	Q7055	CRITICAL	
376S0845	1	SI7149DP	Q7080	CRITICAL	
376S0845	1	SI7149DP	Q7085	CRITICAL	

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT

SYNC_MASTER=JACK_J30 SYNC_DATE=09/27/2013

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

BRANCH:

PAGE: 70 OF 109

SHEET: 64 OF 86

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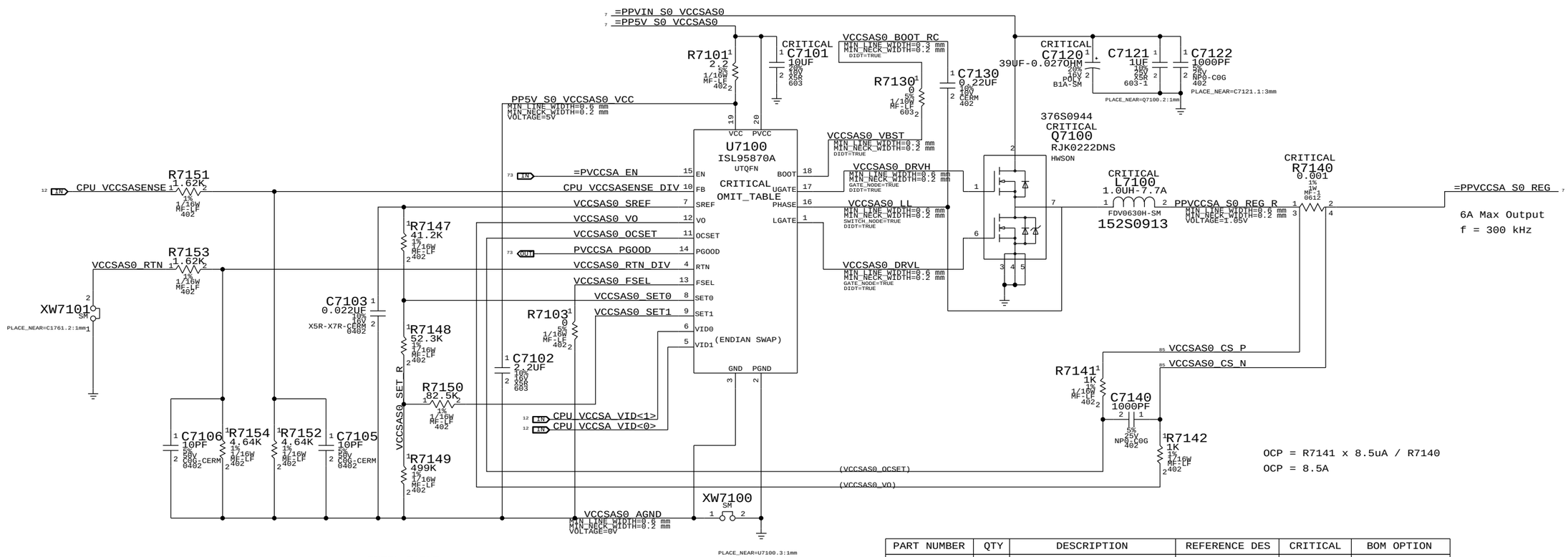
System Agent Power Supply



INTEL TABLE:

VID1	VID0	Voltage
0	0	0.9V
1	0	0.8V
0	1	0.725V
1	1	0.675V

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3074	1	IC,ISL95870A,PWM,2BIT-VID,RMOT-SNSE,20P	U7100	CRITICAL	

SYNC_MASTER=JACK_J30 SYNC_DATE=09/28/2011

PAGE TITLE: System Agent Supply

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

BRANCH:

PAGE: 71 OF 109

SHEET: 65 OF 86

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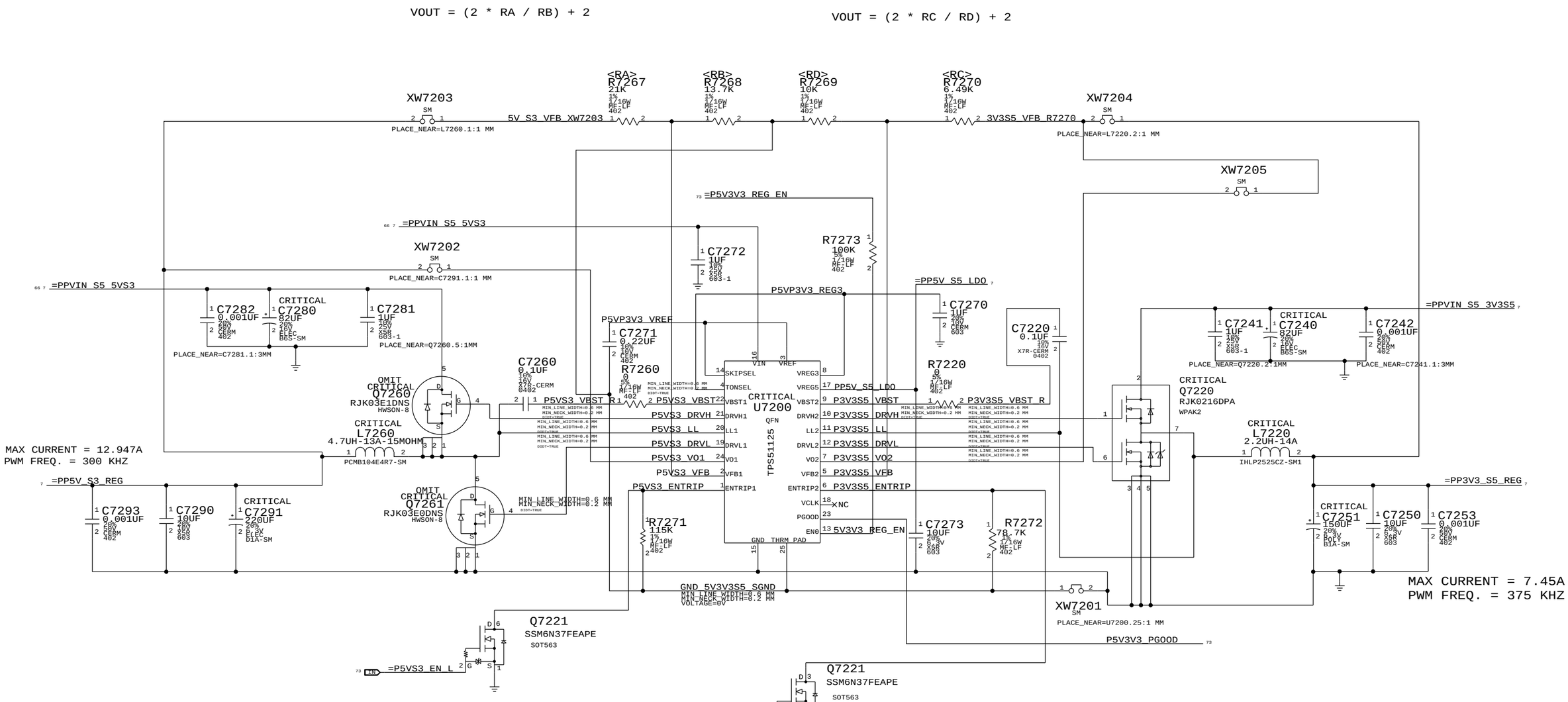
5V_S3/3.3V_S5 POWER SUPPLY



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0927	1	FDMC3020DC	Q7260		5V_S3_POWER_FET:FAIR
376S0928	1	FDMC2514SDC	Q7261		5V_S3_POWER_FET:FAIR
376S0966	1	RJK03E1DNS	Q7260		5V_S3_POWER_FET:REN
376S0895	1	RJK03E0DNS	Q7261		5V_S3_POWER_FET:REN

SYNC_MASTER=JACK_J30 SYNC_DATE=08/22/2011

PAGE TITLE: 5V/3.3V SUPPLY

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

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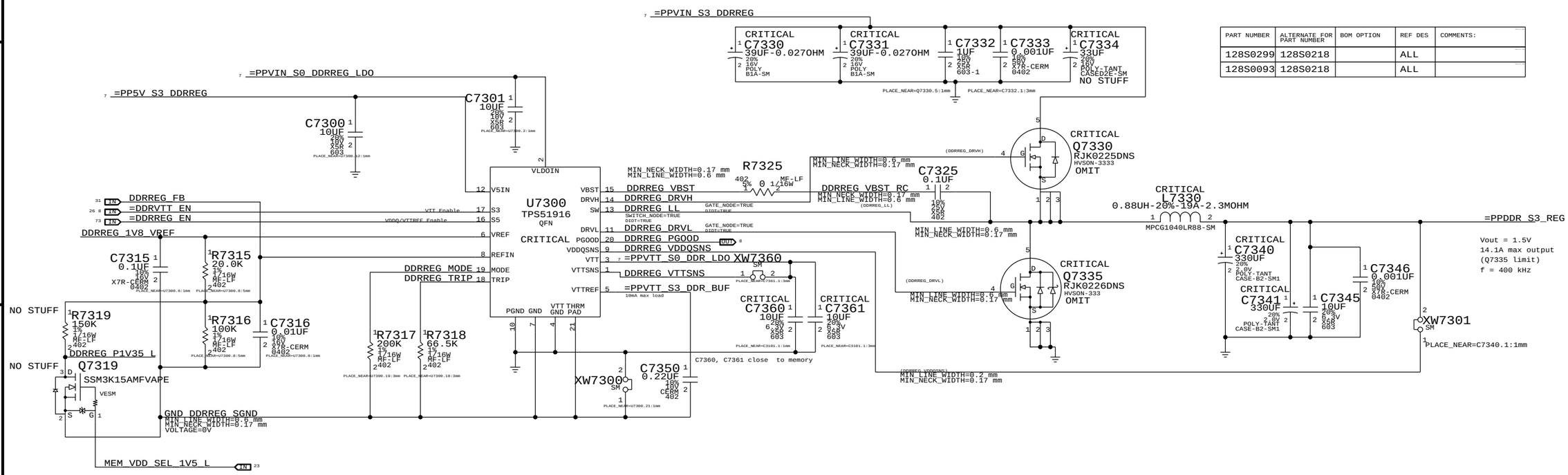

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0979	1	FDMC0225	Q7330		DDR_POWER_FET:FAIR
376S0874	1	FDMC0202S	Q7335		DDR_POWER_FET:FAIR

SYNC_MASTER=JACK_J30 SYNC_DATE=07/28/2011

PAGE TITLE
1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D
REVISION 6.0.0
BRANCH
PAGE 73 OF 109
SHEET 67 OF 86

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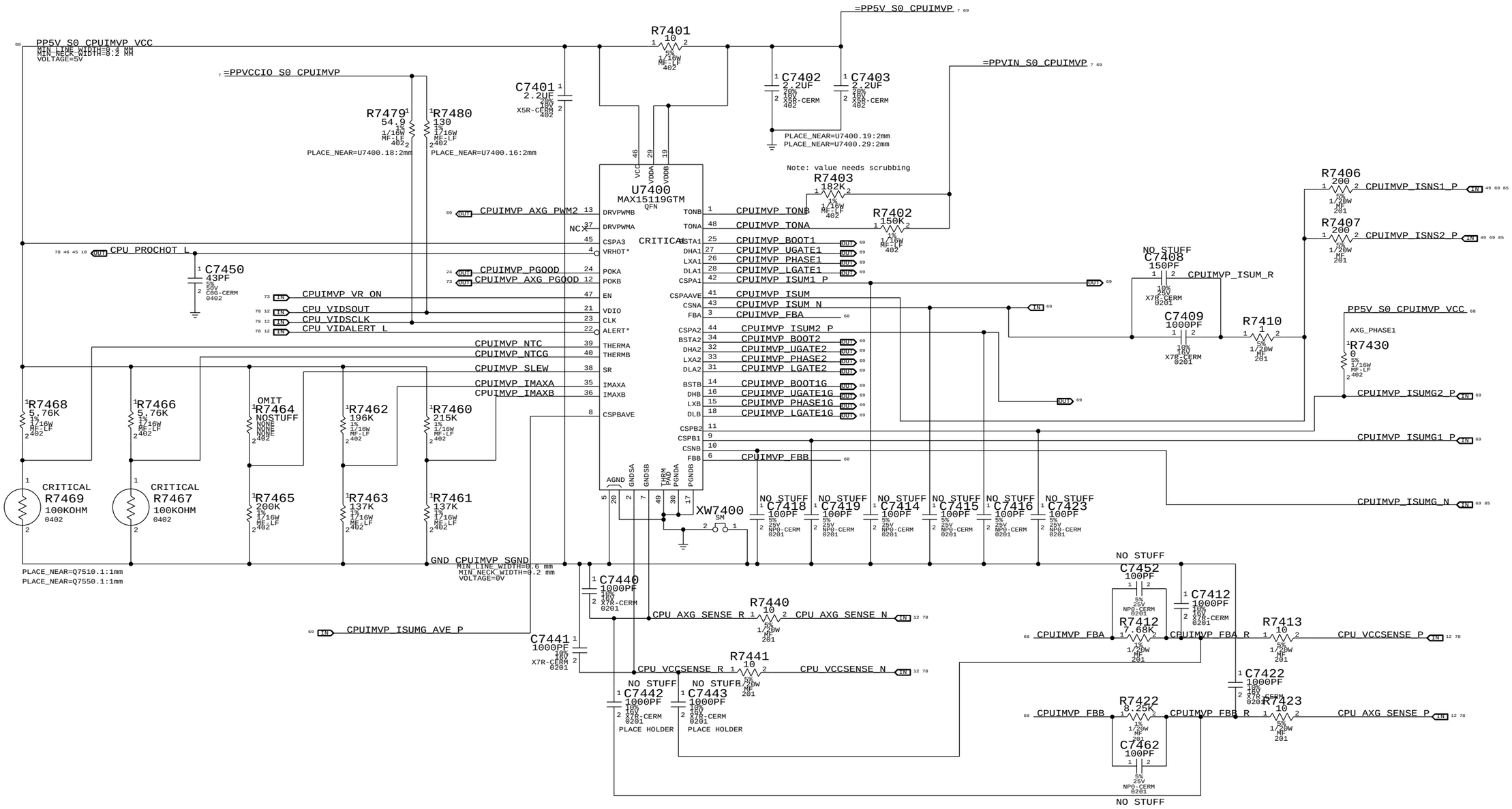

SYNC_MASTER=JACK_J30 SYNC_DATE=08/03/2011

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

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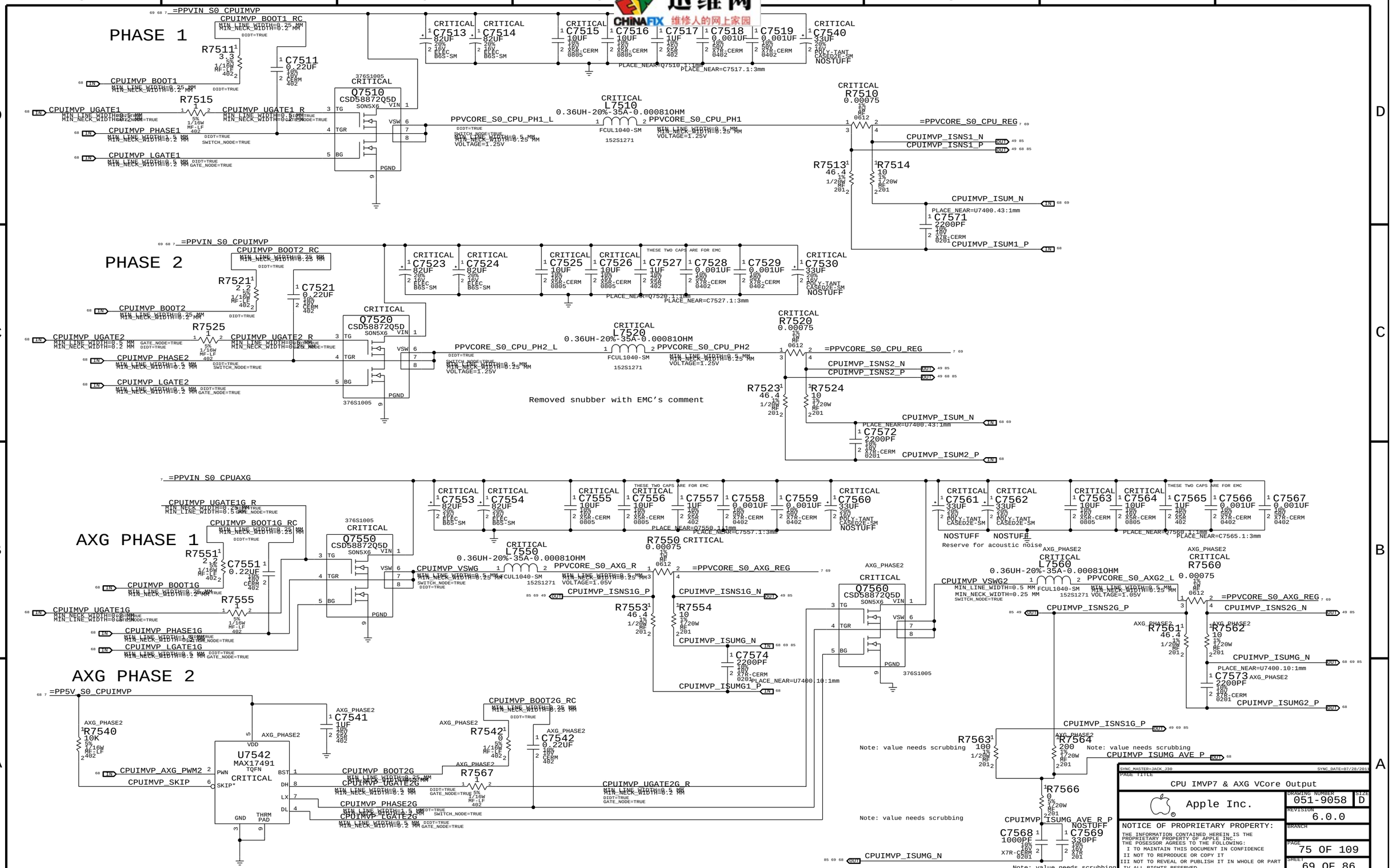

CPU IMVP7 & AXG VCore Output

Apple Inc.

DRAWING NUMBER 051-9058 SIZE D

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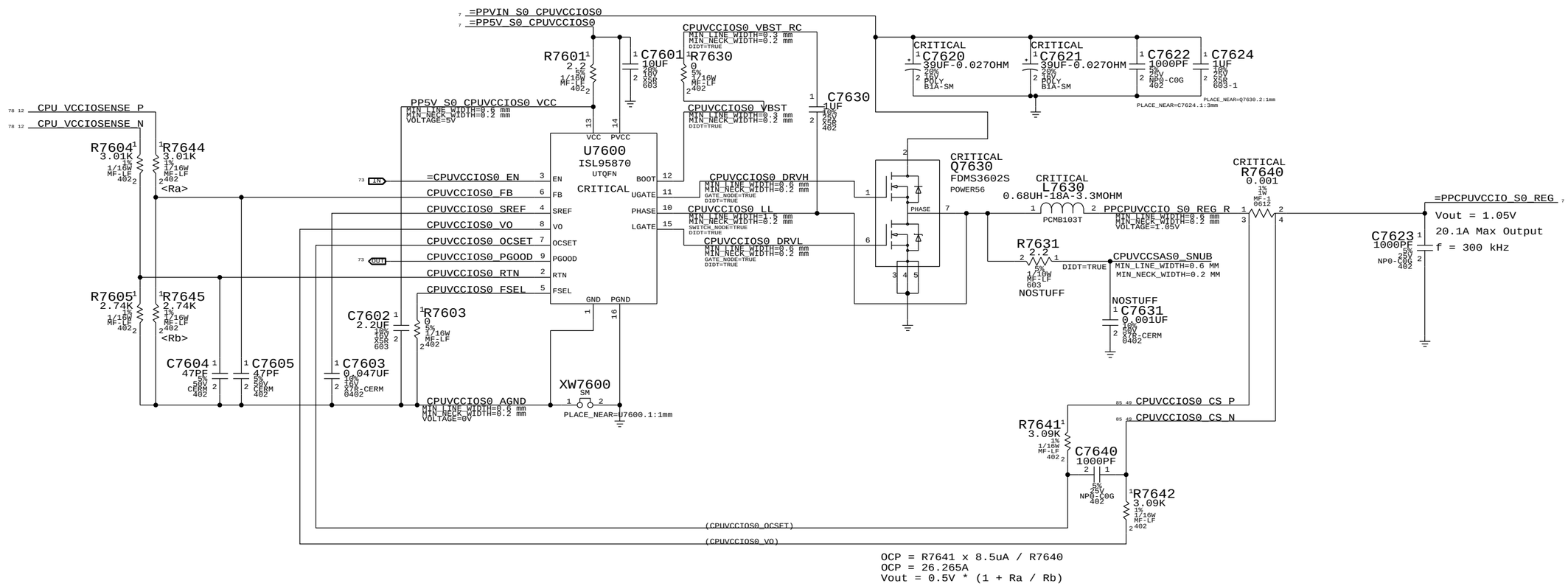
CPU VCCIO (1.05V S0) Regulator



OCP = R7641 x 8.5uA / R7640
OCP = 26.265A
Vout = 0.5V * (1 + Ra / Rb)

SYNC MASTER=JACK J30	SYNC DATE=09/28/2011
PAGE TITLE: CPUVCCIO (1.05V) Power Supply	
Apple Inc.	DRAWING NUMBER: 051-9058 SIZE: D
	REVISION: 6.0.0
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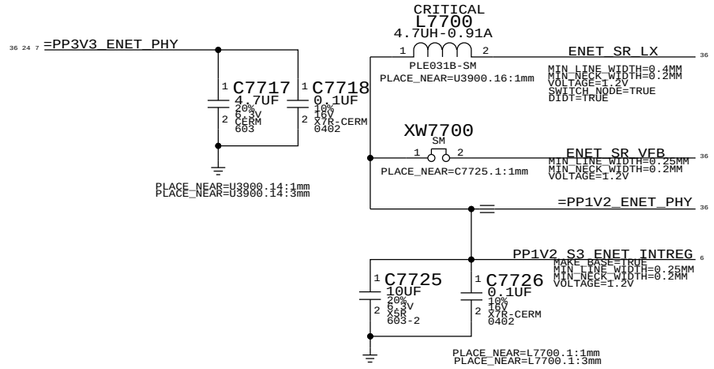
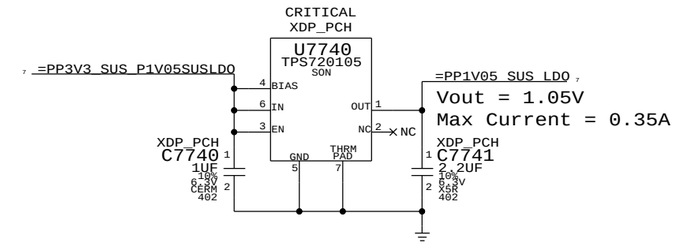
CAESAR IV 1.2V INT.VR CMPTS



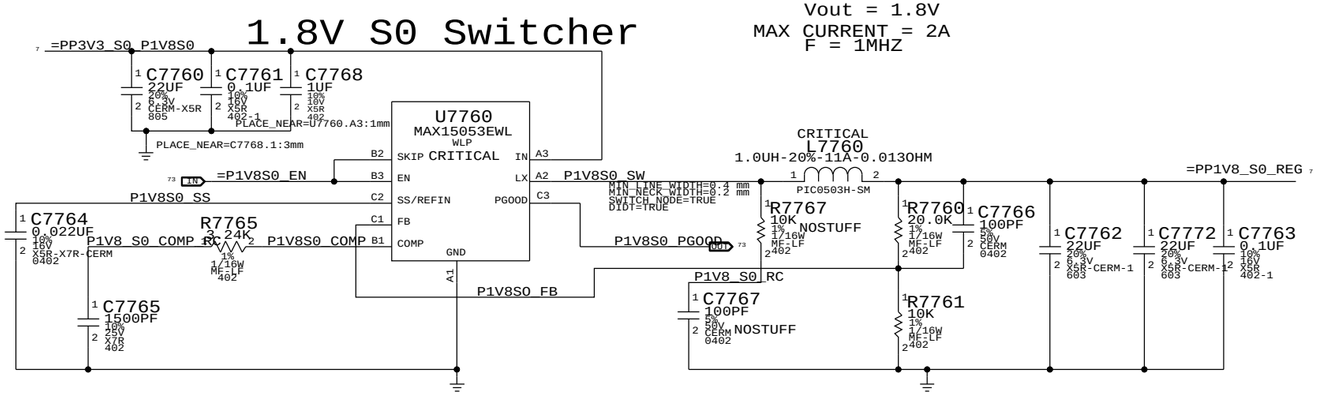
1.05V SUS LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

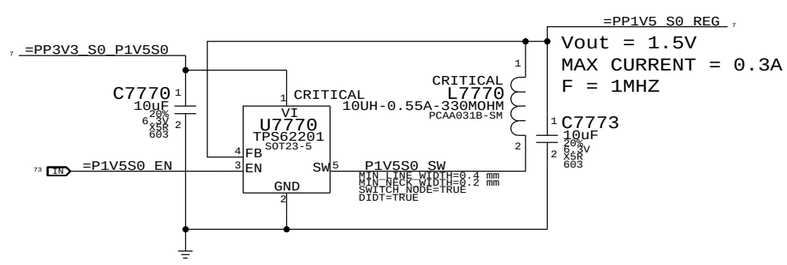


1.8V S0 Switcher

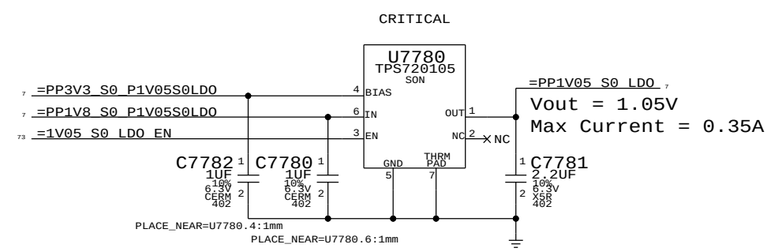
Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



1.5V S0 Switcher



1.05V S0 LDO



SYNC_MASTER=JACK_J30 SYNC_DATE=07/28/2011

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

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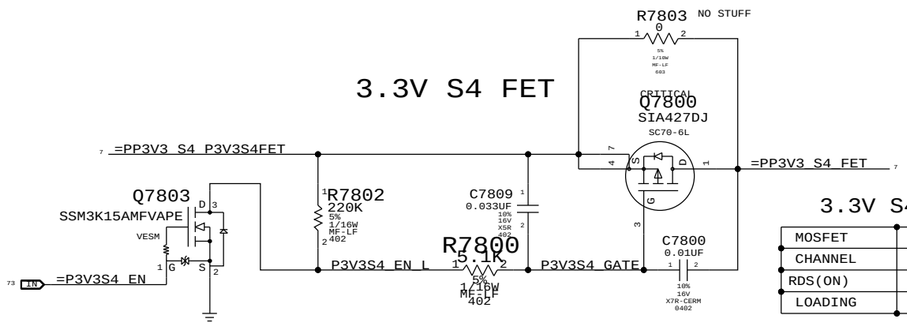
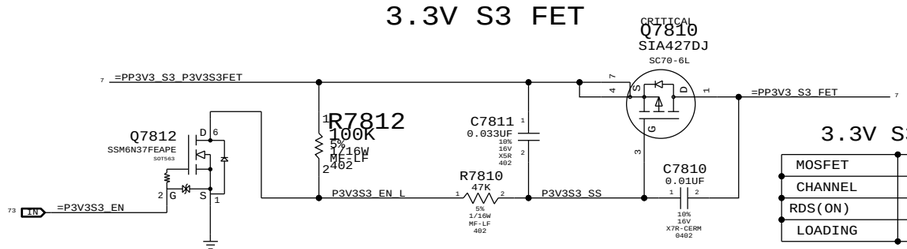
3.3V S4 FET



3.3V S4 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.35 A (EDP)

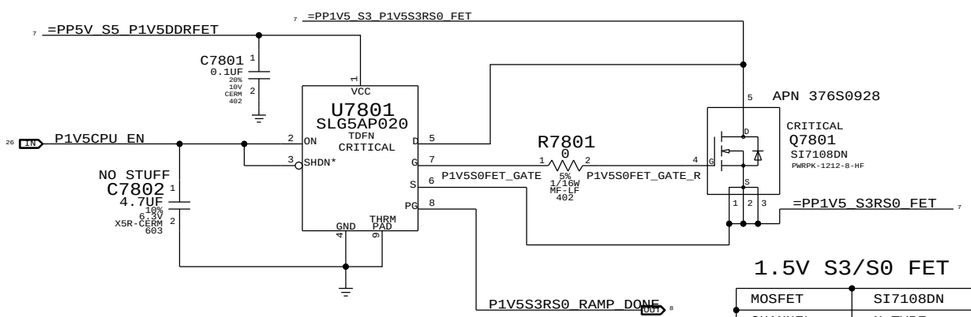
3.3V S3 FET



3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)

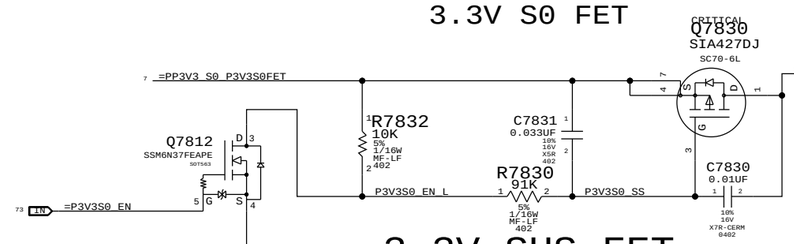
1.5V S3/S0 FET



1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)

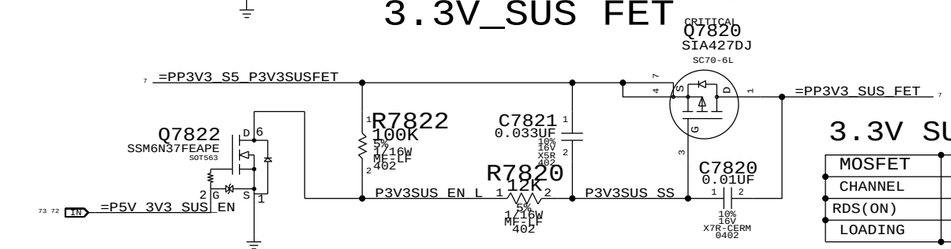
3.3V S0 FET



3.3V S0 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)

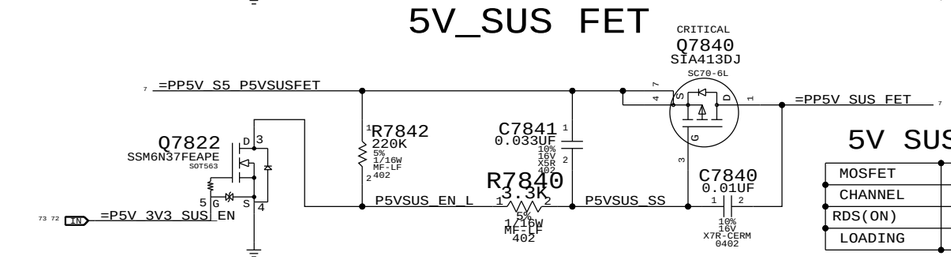
3.3V_SUS FET



3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)

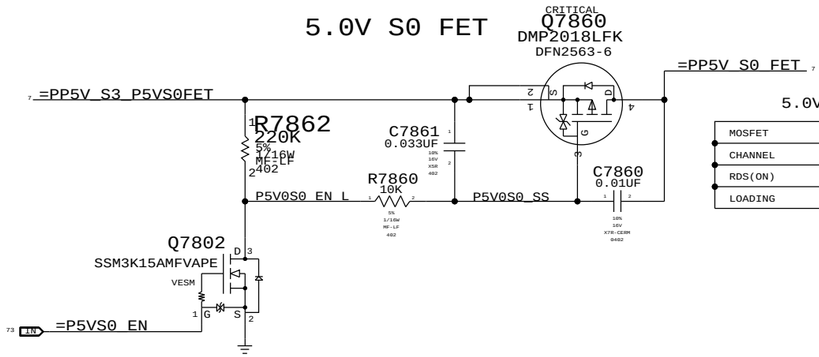
5V_SUS FET



5V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	16 mOhm @4.5V
LOADING	100? mA (EDP)

5.0V S0 FET



5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2011

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

REVISION: 6.0.0

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S5 Rail Enables & PGOOD

=PP3V42_G3H_PWRCTL

Internal pull-ups 100K +/- 20%

C7940 0.1uF 20% 10V CERM 402

U7941 SLG4AP012 TDFN — CRITICAL 34350497

SMC_PM_G2_EN — MAKE_BASE=TRUE

=PP3V3_S5_PWRCTL

Threshold: ??

DLY > 10 ms

S5PGOOD_DLY

C7941 220PF 5% 25V C0G-CERM 0402

R7941 100 5% 1/16W MF-LF 402

C7942 0.033UF 10% 16V X5R 402 NO STUFF

P3V3S5_EN_L — MAKE_BASE=TRUE — =P3V3S5_EN_L

P3V3S5_EN_L_R — MAKE_BASE=TRUE

P5V3V3_REG_EN — MAKE_BASE=TRUE — =P5V3V3_REG_EN

S5_PWRGD — MAKE_BASE=TRUE

S5_PWRGD (old name RSMRST_PWRGD)-->SMC

SMC-->PM_DSW_PWRGD

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

3.3V,5V S3 ENABLE

=PP3V42_G3H_PWRCTL — R7913 68K 5% 1/16W MF-LF 402 — P5V3_EN_L — MAKE_BASE=TRUE — =P5VS3_EN_L

PM_SLP_S4_L — MAKE_BASE=TRUE

R7914 3.3K 5% 1/16W MF-LF 402 — C7913 0.068UF 10% 10V X5R-CERM 0402 — TPAD_VBUS_EN

R7911 5.1K 5% 1/16W MF-LF 402 — R7912 9.1K 5% 1/16W MF-LF 402 — Q7911 SSM3K15AMFVAPE VESM

PLACE_NEAR=U5701.3:6mm — PLACE_NEAR=Q7812.2:6mm — PLACE_NEAR=U7300.16:6mm

P3V3S3_EN — MAKE_BASE=TRUE — =P3V3S3_EN

DDRREG_EN — MAKE_BASE=TRUE — =DDRREG_EN

=USB_PWR_EN

C7910 0.47UF 10% 6.3V CERM-X5R 402 — C7912 0.47UF 10% 6.3V CERM-X5R 402

PLACE_NEAR=U7300.16:6mm — PLACE_NEAR=Q7812.2:6mm

3.3V S4 ENABLE

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7970.6:3mm — C7970 0.1UF 10% 10V X5R-CERM 0201

PM_SLP_S5_L — U7970 74LVC1G32 SOT891 — P3V3_S4_EN — MAKE_BASE=TRUE — =P3V3S4_EN — =TBTAPWRSW_EN

SMC_S4_WAKESRC_EN — NC — NO STUFF R7919 0 5% 1/16W MF-LF 402 — PLACE_NEAR=U1800.G18:5mm

S0 ENABLE

PM_SLP_S3_L — R7978 100 5% 1/16W MF-LF 402 — (PM_SLP_S3_R_L) — PM_SLP_S3_R_L — MAKE_BASE=TRUE

R7987 33K 5% 1/16W MF-LF 402 — R7981 20K 5% 1/16W MF-LF 402 — R7988 39K 5% 1/16W MF-LF 402 — R7986 5.1K 5% 1/16W MF-LF 402

PLACE_NEAR=U7100.15:6mm — PLACE_NEAR=U7600.3:6mm — PLACE_NEAR=U7770.3:6mm — PLACE_NEAR=U7760.83:6mm

=P5VS0_EN — =P3V3S0_EN — =PBUSVSENS_EN — P1V8S0_EN — MAKE_BASE=TRUE — =P1V8S0_EN — P1V5S0_EN — MAKE_BASE=TRUE — =P1V5S0_EN — =1V05_S0_LDO_EN — CPUVCCIOS0_EN — MAKE_BASE=TRUE — =CPUVCCIOS0_EN — PVCCSA_EN — MAKE_BASE=TRUE — =PVCCSA_EN

C7987 0.47UF 10% 6.3V CERM-X5R 402 — C7981 0.47UF 10% 6.3V CERM-X5R 402 — C7988 0.47UF 10% 6.3V CERM-X5R 402 — C7986 0.47UF 10% 6.3V CERM-X5R 402

CPUVCORE ENABLE

ALL_SYS_PWRGD — R7974 0 5% 1/16W MF-LF 402 — PLACE_NEAR=U7400.7:5mm — CPUIMVP_VR_ON

3.3V/5.0V Sus ENABLE

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7940.1:2.3mm — C7943 0.1uF 20% 10V CERM 402

SMC_BATLOW_L:100K pull up on SMC page — SMC_BATLOW_L — ALL_SYS_PWRGD — PM_SLP_SUS_L — U7940 74AUP1G32GS SOT891 — PM_SUS_EN — MAKE_BASE=TRUE — =P5V_3V3_SUS_EN

NO STUFF R7917 0 5% 1/16W MF-LF 402

=PP3V42_G3H_PWRCTL — R7931 10K 5% 1/16W MF-LF 402 — CHGR_VFRQ

Q7931 SSM3K15AMFVAPE VESM

CHGR VFRQ Generation

VFRQ Low: Fix Frequency

VFRQ High: Variable Frequency

S0 Rail PGOOD (BJT Version)

=PP3V3_S0_VMON — R7951 15.0K 1% 1/16W MF-LF 402 — R7952 7.15K 1% 1/16W MF-LF 402

=PP3V3_S5_VMON — R7956 150K 1% 1/10W MF-LF 402 — S0PGD_C

VMON_3V3_DIV — R7953 1K 5% 1/10W MF-LF 402 — VMON_Q2_BASE

=PP1V5_S0_VMON — PP1V5_S0 — R7954 1K 5% 1/10W MF-LF 402 — VMON_Q3_BASE

=PP1V05_S0_VMON — R7955 1K 5% 1/10W MF-LF 402 — VMON_Q4_BASE

Q7950 ASMCC0179 DFN2015H4-8 — CRITICAL — NC — NC

353S2809 — S0PGD_BJT_GND_R

R7957 100 5% 1/10W MF-LF 402

Worst-Case Thresholds:

Q2: 0.XXXV

Q3: 0.640V

3.3V w/Divider: 2.345V

Q4: 0.660V

3.3V SUS Detect

=PP3V3_S5_PWRCTL — PLACE_NEAR=U7930.6:2.3mm — C7930 0.1uF 20% 10V CERM 402

No stuff C7931, 12ms Min delay time'

U7930 Sense input threhold is 3.07V

=PP3V3_SUS_PWRCTL — R7933 100K 5% 1/10W MF-LF 402

CRITICAL — U7930 TPS3808G33DBVRG4 SOT23-6 — PM_RSMRST_L — PM_RSMRST_L goes to U1800.C21

S4_PGOOD_CT — C7931 0.001UF 10% 16V CERM 402 NO STUFF

ENET Enable Generation

"ENET" = "S0" || ("S3" && "AC" && "WOL_EN")

3.3V ENET FET

CRITICAL Q7922 NTR4101P SOT-23-HF

=PP3V3_S3_P3V3ENETFET — =PP3V3_ENET_FET

R7921 10K 5% 1/16W MF-LF 402 — C7921 0.033UF 10% 16V X5R 402 — R7922 100K 5% 1/16W MF-LF 402 — C7922 0.01UF 10% 16V X7R-CERM 0402

PM_ENET_EN_L — P3V3ENET_SS

Q7925 2N7002DW-X-G SOT-363 — WOL_EN

WLAN Enable Generation

"WLAN" = ("S3" && "AP_PWR_EN" && ("AC" || "S0"))

NOTE: S3 term is guaranteed by S3 pull-up on open-drain AP_PWR_EN signal.

PM_WLAN_EN_L — Q7925 2N7002DW-X-G SOT-363 — AP_PWR_EN

Q7921 SSM3K15AMFVAPE VESM — PM_SLP_S3_L

Q7920 2N7002DW-X-G SOT-363 — AC_EN_L — (AC_EN_L) — NO STUFF R7929 0 5% 1/10W MF-LF 402 — SMC_ADAPTER_EN — (PM_SLP_S3_L)

S0 Rail PGOOD Circuitry

(ISL Version in development)

Thresholds:

VDD: 2.734V-3.010V

V2MON: 2.815V-3.099V

V3MON: 0.572V-0.630V

V4MON: 0.572V-0.630V

=PP5V_S0_VMON — =PP1V5_S0_VMON — =PP1V05_S0_VMON — =PP3V3_S0_VMON

S0PGOOD_ISL — R7960 6.04K 1% 1/16W MF-LF 402 — R7970 10K 1% 1/16W MF-LF 402 — R7972 6.04K 1% 1/16W MF-LF 402

C7960 0.1uF 20% 10V CERM 402

U7960 ISL88042IRTEZ TDFN (TRU) — CRITICAL — NC — NC

P5V_DIV_VMON — P1V5_DIV_VMON — P1V05_DIV_VMON

R7961 15.0K 1% 1/16W MF-LF 402 — R7971 10K 1% 1/16W MF-LF 402 — R7973 15.0K 1% 1/16W MF-LF 402

353S2310

P1V5S0_PGOOD from U7710

R7967 10K 5% 1/16W MF-LF 402

R7968 100 5% 1/16W MF-LF 402 NO STUFF — CPUIMVP_AXG_PGOOD

R7966 100 5% 1/16W MF-LF 402 — P1V8S0_PGOOD

R7965 100 5% 1/16W MF-LF 402 — P5V3V3_PGOOD

R7964 100 5% 1/16W MF-LF 402 — CPUVCCIOS0_PGOOD

R7963 100 5% 1/16W MF-LF 402 — PVCCSA_PGOOD

ALL_SYS_PWRGD_R — R7962 330 5% 1/16W MF-LF 402 — ALL_SYS_PWRGD

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SYNC MASTER=K90I_MLB — SYNC DATE=02/15/2011

PAGE TITLE: Power Control 1/ENABLE

Apple Inc.

DRAWING NUMBER: 051-9058 — SIZE: D

REVISION: 6.0.0

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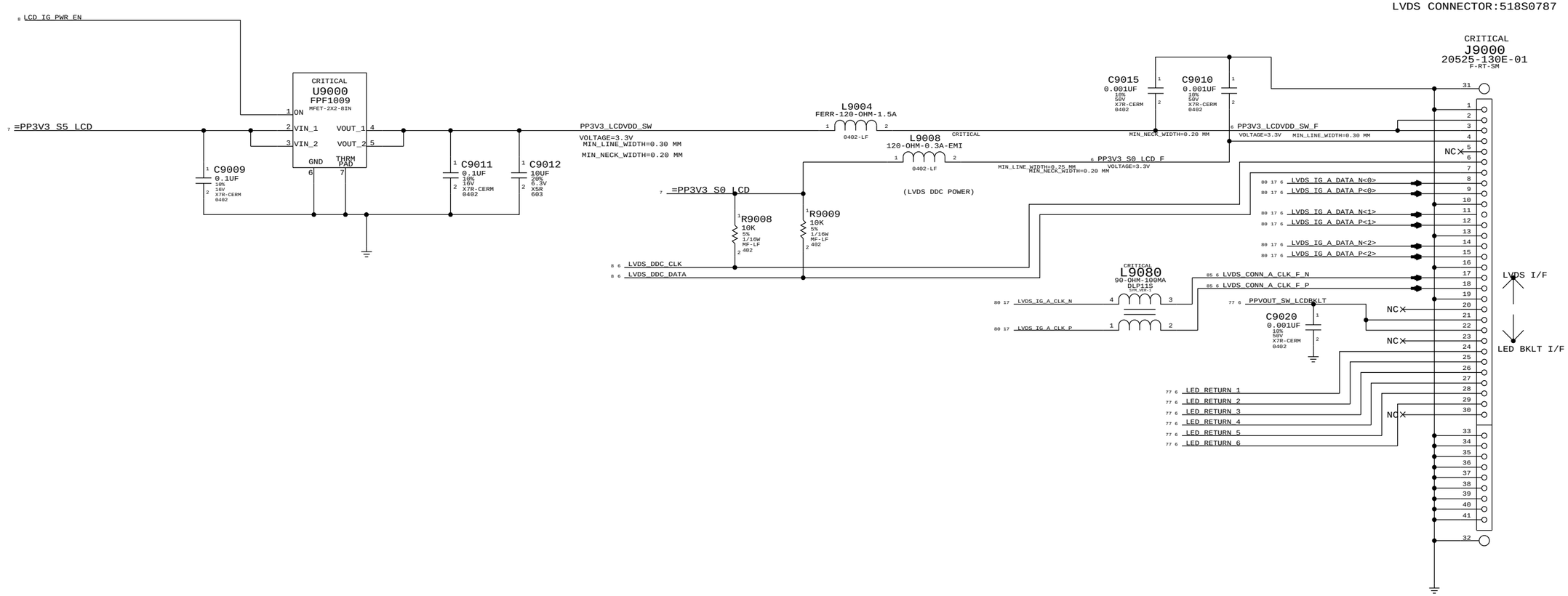
LCD CONNECTOR

LVDS CONNECTOR:518S0787



SYNC_MASTER=K90I_MLB	SYNC_DATE=02/15/2011
PAGE TITLE: LVDS CONNECTOR	
Apple Inc.	DRAWING NUMBER: 051-9058 SIZE: D
	REVISION: 6.0.0
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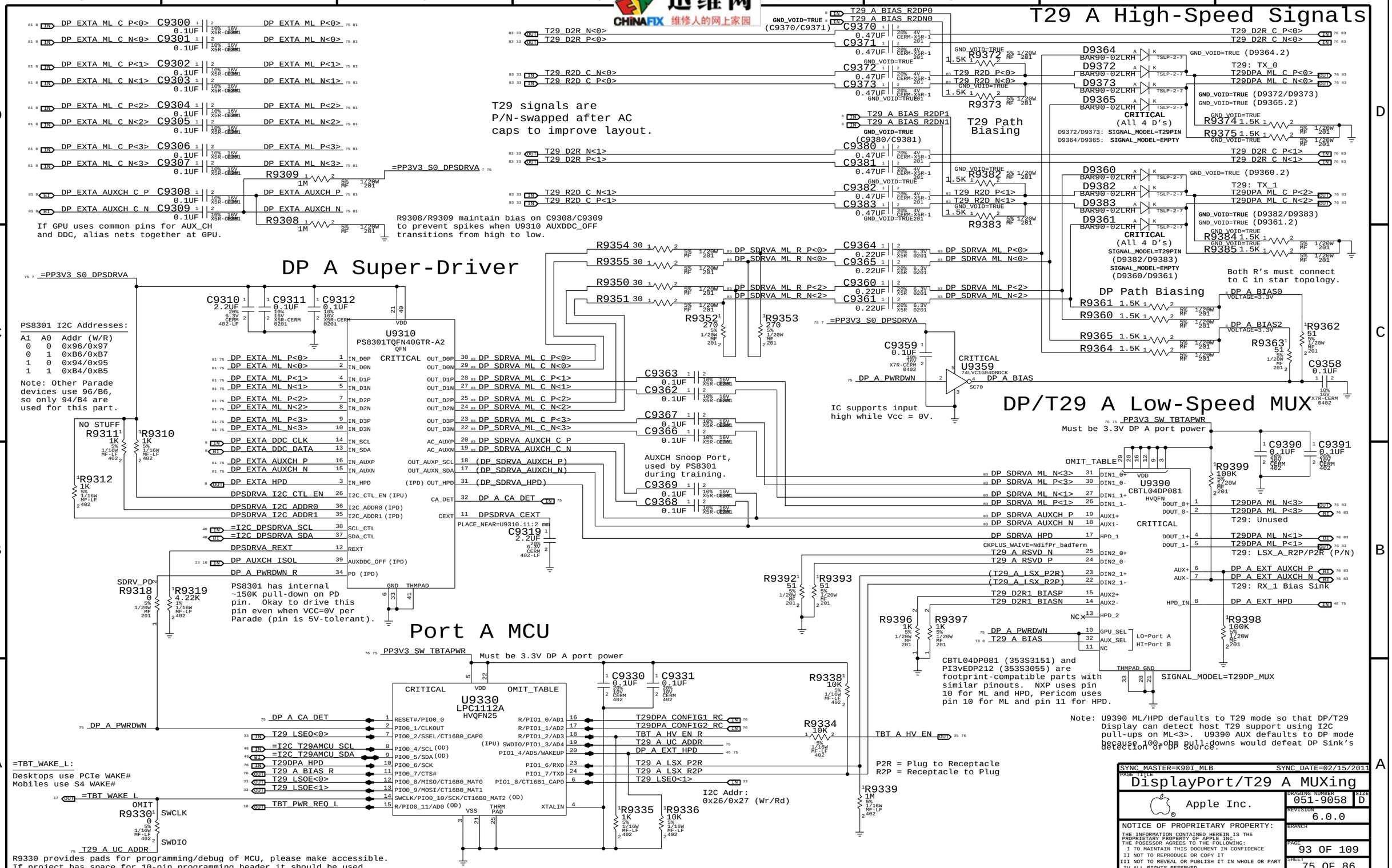
T29 A High-Speed Signals
DP A Super-Driver
DP/T29 A Low-Speed MUX
Port A MCU
T29 signals are P/N-swapped after AC caps to improve layout.
T29 Path Biasing
DP Path Biasing
If GPU uses common pins for AUX_CH and DDC, alias nets together at GPU.
R9308/R9309 maintain bias on C9308/C9309 to prevent spikes when U9310 AUXDDC_OFF transitions from high to low.
PS8301 I2C Addresses:
A1 A0 Addr (W/R)
0 0 0x96/0x97
0 1 0xB6/0xB7
1 0 0x94/0x95
1 1 0xB4/0xB5
Note: Other Parade devices use 96/B6, so only 94/B4 are used for this part.
U9310
PS8301TQFN40GTR-A2
QFN
CRITICAL
PS8301 has internal ~150K pull-down on PD pin. Okay to drive this pin even when VCC=0V per Parade (pin is 5V-tolerant).
AUXCH Snoop Port, used by PS8301 during training.
IC supports input high while Vcc = 0V.
U9359
74LVC1G04DBDCK
U9390
CBTL04DP081
HVQFN
OMIT_TABLE
Must be 3.3V DP A port power
T29: Unused
T29: LSX_A_R2P/P2R (P/N)
T29: RX_1 Bias Sink
CBTL04DP081 (353S3151) and PI3vEDP212 (353S3055) are footprint-compatible parts with similar pinouts. NXP uses pin 10 for ML and HPD, Pericom uses pin 10 for ML and pin 11 for HPD.
Both R's must connect to C in star topology.
SIGNAL_MODEL=T29DP_MUX
Note: U9390 ML/HPD defaults to T29 mode so that DP/T29 Display can detect host T29 support using I2C pull-ups on ML<3>. U9390 AUX defaults to DP mode because 100 ohm pull-downs would defeat DP Sink's detection of DP Source.
U9330
LPC1112A
HVQFN25
=TBT_WAKE_L:
Desktops use PCIe WAKE#
Mobile use S4 WAKE#
R9330 provides pads for programming/debug of MCU, please make accessible.
If project has space for 10-pin programming header it should be used.
P2R = Plug to Receptacle
R2P = Receptacle to Plug
I2C Addr: 0x26/0x27 (Wr/Rd)
SYNC MASTER=K90I_MLB
SYNC DATE=02/15/2011
PAGE TITLE
DisplayPort/T29 A MUXing
Apple Inc.
DRAWING NUMBER 051-9058
SIZE D
REVISION 6.0.0
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PAGE 93 OF 109
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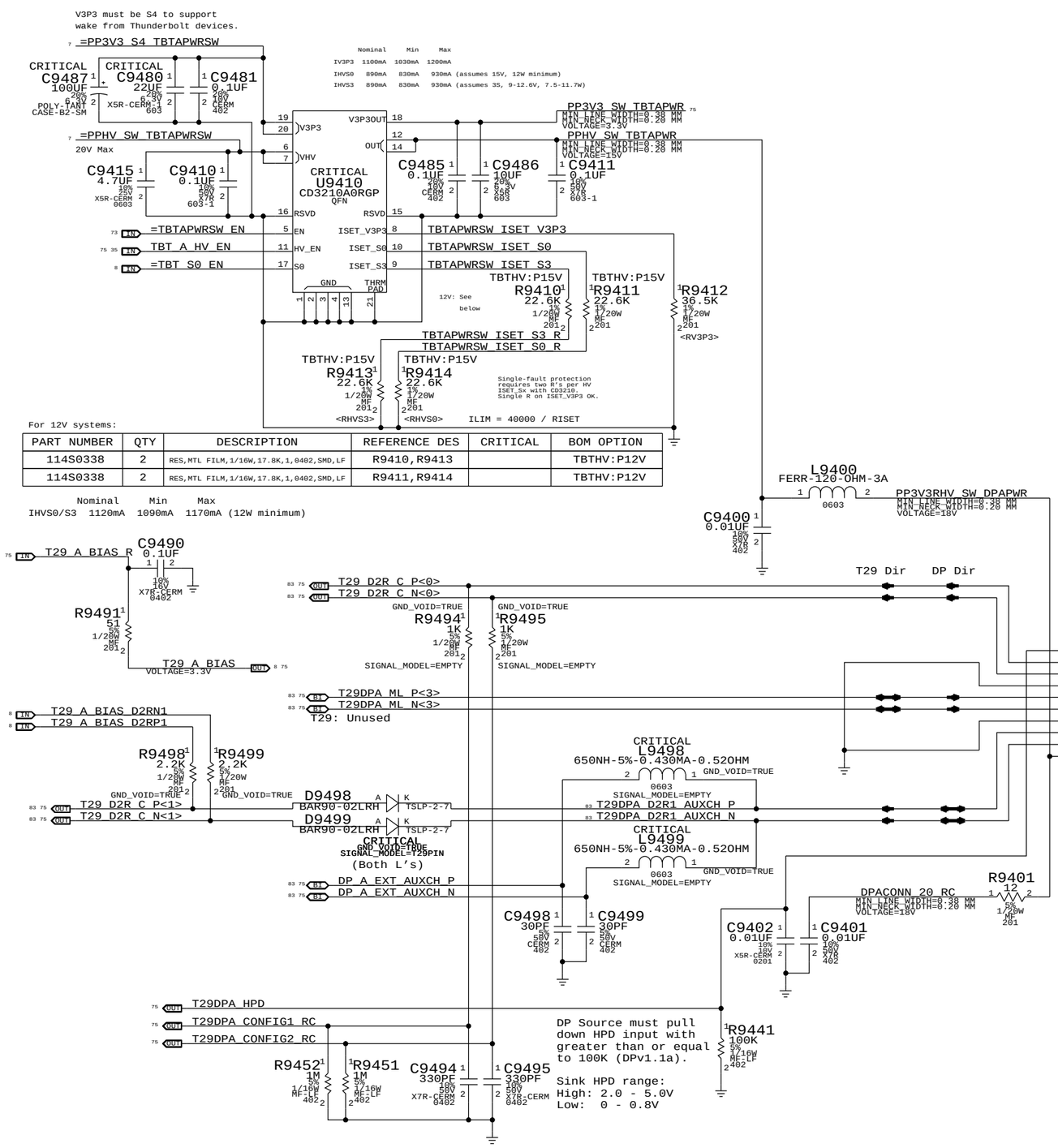
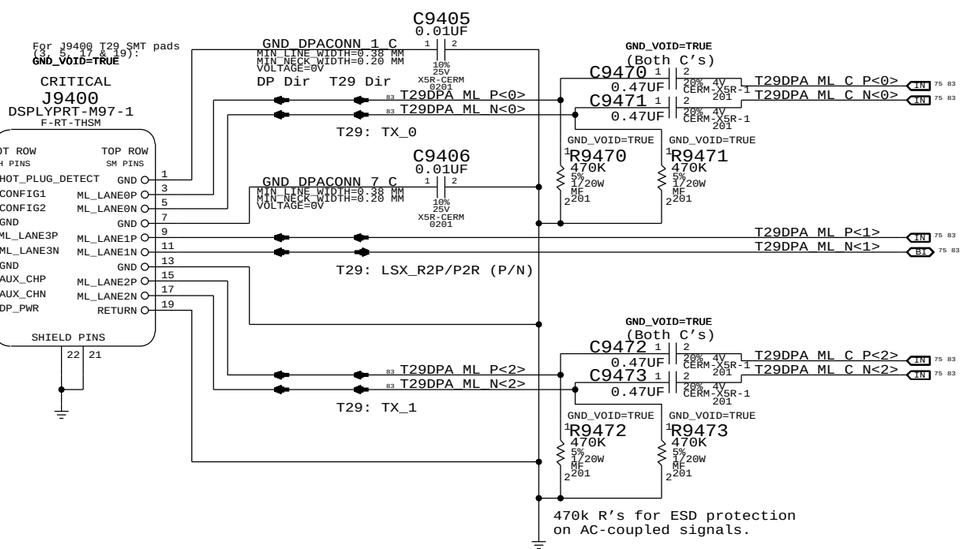
3.3V/HV Power MUX



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9410,R9413		TBTHV:P12V
114S0338	2	RES,MTL FILM,1/16W,17.8K,1,0402,SMD,LF	R9411,R9414		TBTHV:P12V

Thunderbolt Connector A



SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE: Thunderbolt Connector A

Apple Inc.

DRAWING NUMBER: 051-9058 SIZE: D

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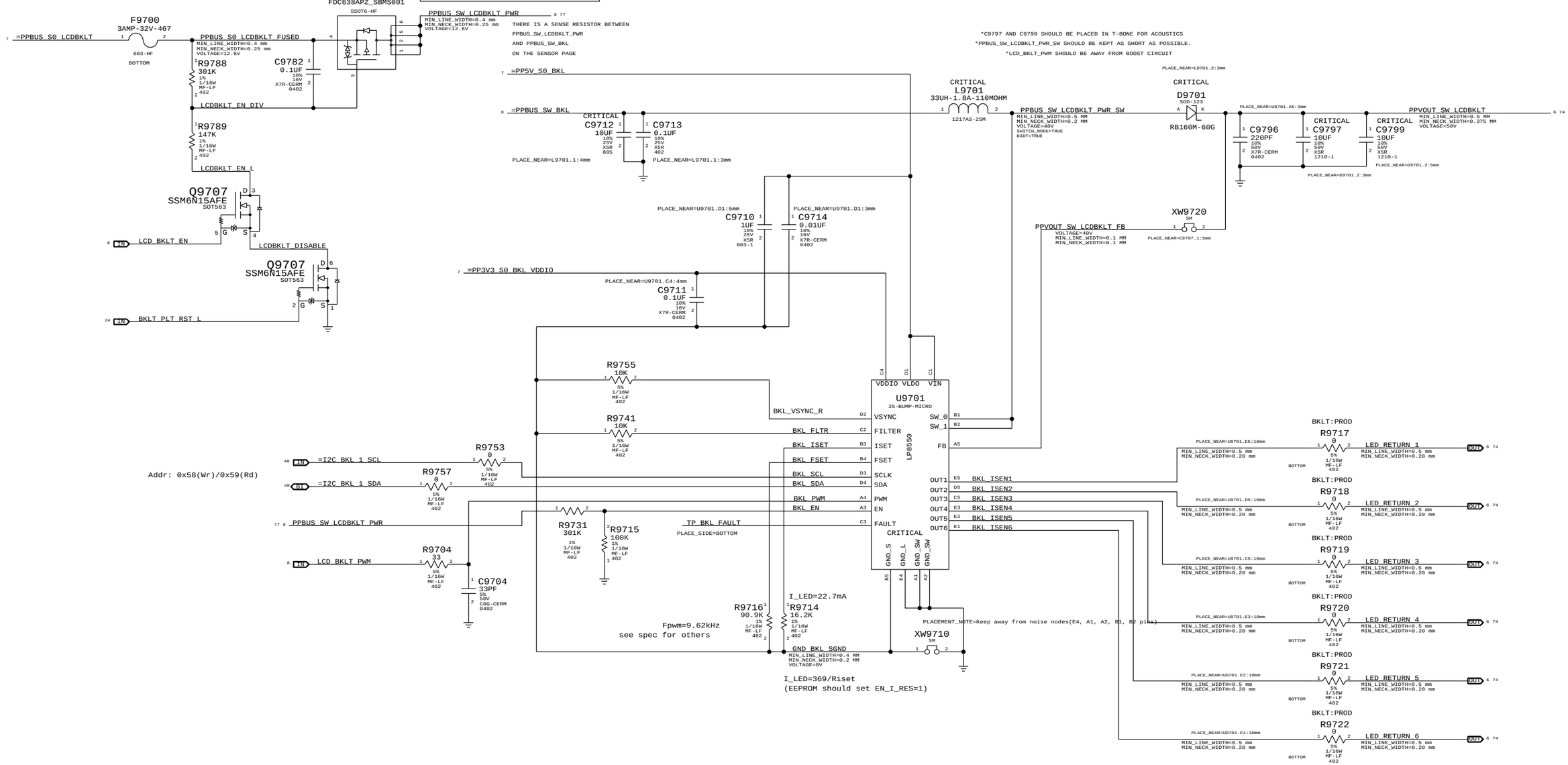
PPBUS S0 LCDBKLT FET

MOSFET	FDC638APZ
CHANNEL	P-TYPE
RDS(ON)	43 mOhm @4.5V
LOADING	0.715 A (EDP)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMR9717,R9718,R9719			BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SMR9720,R9721,R9722			BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC_MASTER=J31_MLB SYNC_DATE=07/08/2011

PAGE TITLE
LCD Backlight Driver

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_PCH_TX2TX	*	=3X_DIELECTRIC	?
PCIE_PCH_TX2RX	*	=4X_DIELECTRIC	?
PCIE_PCH_RX2RX	*	=3x_DIELECTRIC	?
PCIE_PCH_RX2TX	*	=4x_DIELECTRIC	?
PCIE_PCH_2OTHER	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_PCH_TX2TX	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_PCH_TX2RX	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_PCH_RX2RX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_PCH_RX2TX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_PCH_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	*_PCH_TX	*	PCIE_PCH_TX2TX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_PCH_TX2RX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_PCH_RX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_PCH_RX2TX
PCIE_PCH_TX	*	*	PCIE_PCH_2OTHER
PCIE_PCH_RX	*	*	PCIE_PCH_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

operties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE_PCH_TX	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_85D	PCIE_PCH_TX	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE_PCH_RX	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE_PCH_RX	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE_PCH_RX	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE_PCH_RX	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	CPU_COMP	CPU_PECI	10 19 46
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 26
	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 24
	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10 45
	CPU_50S	CPU_AGTL	CPU_VCCIO_SEL	8 12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 45 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19 46
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_R_L	CPU_50S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 70
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 68
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 68
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
CPU_SVIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L	12 68
CPU_SVIDSCLK	CPU_50S	CPU_COMP	CPU_VIDSCLK	12 68
CPU_SVIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT	12 68

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

PAGE TITLE
CPU Constraints

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DRAWING NUMBER 051-9058 SIZE D
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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL10	N	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL10	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines
per Huron River SFF DG rev1.0 (#438297).
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQ to DQS matching per byte lane should be within 0.127mm.
DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.
SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	11 27
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	11 27
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11 28
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11 28
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11 28
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11 28
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11 28
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11 28
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11 28
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	11 28

SYNC MASTER=K90I_MLB SYNC DATE=02/15/2013

PAGE TITLE
Memory Constraints

Apple Inc.

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_PCH	*	=3x_DIELECTRIC	?
DP_PCH_TX	*	=3x_DIELECTRIC	?
LVDS_PCH_TX	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_PCH	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_PCH_TX	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS_PCH_TX	TOP,BOTTOM	=4x_DIELECTRIC	?

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_PCH_TX	*	=3x_DIELECTRIC	?
SATA_PCH_RX	*	=3x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_PCH_TX	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_PCH_RX	TOP,BOTTOM	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_PCH_TX2TX	*	=4X_DIELECTRIC	?
SATA3_PCH_TX2RX	*	=5X_DIELECTRIC	?
SATA3_PCH_RX2RX	*	=4x_DIELECTRIC	?
SATA3_PCH_RX2TX	*	=5x_DIELECTRIC	?
SATA3_PCH_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA3_PCH_TX2TX	TOP,BOTTOM	=5X_DIELECTRIC	?
SATA3_PCH_TX2RX	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA3_PCH_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
SATA3_PCH_RX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
SATA3_PCH_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA3_PCH_TX	*_PCH_TX	*	SATA3_PCH_TX2TX
SATA3_PCH_TX	*_PCH_RX	*	SATA3_PCH_TX2RX
SATA3_PCH_RX	*_PCH_RX	*	SATA3_PCH_RX2RX
SATA3_PCH_RX	*_PCH_TX	*	SATA3_PCH_RX2TX
SATA3_PCH_TX	*	*	SATA3_PCH_2OTHER
SATA3_PCH_RX	*	*	SATA3_PCH_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

USB 3.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX2TX	*	=4X_DIELECTRIC	?
USB3_PCH_TX2RX	*	=5X_DIELECTRIC	?
USB3_PCH_RX2RX	*	=4x_DIELECTRIC	?
USB3_PCH_RX2TX	*	=5x_DIELECTRIC	?
USB3_PCH_2OTHER	*	=4x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_PCH_TX2TX	TOP,BOTTOM	=5X_DIELECTRIC	?
USB3_PCH_TX2RX	TOP,BOTTOM	=6X_DIELECTRIC	?
USB3_PCH_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
USB3_PCH_RX2TX	TOP,BOTTOM	=6x_DIELECTRIC	?
USB3_PCH_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_PCH_TX	*_PCH_TX	*	USB3_PCH_TX2TX
USB3_PCH_TX	*_PCH_RX	*	USB3_PCH_TX2RX
USB3_PCH_RX	*_PCH_RX	*	USB3_PCH_RX2RX
USB3_PCH_RX	*_PCH_TX	*	USB3_PCH_RX2TX
USB3_PCH_TX	*	*	USB3_PCH_2OTHER
USB3_PCH_RX	*	*	USB3_PCH_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

operties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	LVDS_IG_A_CLK	LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_CLK_P	17 74
	LVDS_IG_A_CLK	LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_CLK_N	17 74
	LVDS_IG_A_DATA	LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_DATA_P<2..0>	6 17 74
	LVDS_IG_A_DATA	LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_DATA_N<2..0>	6 17 74
		LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_DATA_P<3>	8 17
		LVDS_90D	LVDS_PCH_TX	LVDS_IG_A_DATA_N<3>	8 17
		LVDS_90D	LVDS_PCH_TX	LVDS_IG_B_DATA_P<3..0>	8 17
		LVDS_90D	LVDS_PCH_TX	LVDS_IG_B_DATA_N<3..0>	8 17
		LVDS_90D	LVDS_PCH_TX	LVDS_IG_B_CLK_P	8 17
		LVDS_90D	LVDS_PCH_TX	LVDS_IG_B_CLK_N	8 17
	SATA_HDD_R2D	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_C_P	16 41
	SATA_HDD_R2D	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_C_N	16 41
	SATA_HDD_R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_P	6 41
	SATA_HDD_R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_N	6 41
	SATA_HDD_D2R	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_P	16 41
	SATA_HDD_D2R	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_N	16 41
	SATA_HDD_D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_C_P	6 41
	SATA_HDD_D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_C_N	6 41
	SATA_ODD_R2D	SATA_90D	SATA_PCH_TX	SATA_ODD_R2D_C_P	16 41
	SATA_ODD_R2D	SATA_90D	SATA_PCH_TX	SATA_ODD_R2D_C_N	16 41
	SATA_ODD_R2D	SATA_90D	SATA_PCH_TX	SATA_ODD_R2D_P	6 41
	SATA_ODD_R2D	SATA_90D	SATA_PCH_TX	SATA_ODD_R2D_N	6 41
	SATA_ODD_D2R	SATA_90D	SATA_PCH_RX	SATA_ODD_D2R_P	16 41
	SATA_ODD_D2R	SATA_90D	SATA_PCH_RX	SATA_ODD_D2R_N	16 41
	SATA_HDD_R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RC_P	41
	SATA_HDD_R2D_CONN	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RC_N	41
	SATA_HDD_D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_RC_P	41
	SATA_HDD_D2R_CONN	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_RC_N	41
	PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
	USB_HUB1_UP	USB_85D	USB	USB_HUB_UP_P	18 25
		USB_85D	USB	USB_HUB_UP_N	18 25
	USB_EXTA	USB_85D	USB	USB_EXTA_P	18 42
	USB_EXTA	USB_85D	USB	USB_EXTA_N	18 42
	USB_EXTB	USB_85D	USB	USB_EXTB_MUX_P	25 43
		USB_85D	USB	USB_EXTB_MUX_N	25 43
1219		USB_85D	USB	USB_EXTA_MUXED_F_P	42
1220		USB_85D	USB	USB_EXTA_MUXED_F_N	42
1221		USB_85D	USB	USB_EXTB_F_P	43
1222		USB_85D	USB	USB_EXTB_F_N	43
1223		USB_85D	USB	USB_EXTA_MUXED_P	42
1224		USB_85D	USB	USB_EXTA_MUXED_N	42
1225		USB_85D	USB	USB_EXTD_XHCI_P	8 18
1226		USB_85D	USB	USB_EXTD_XHCI_N	8 18
1247		USB_85D	USB	USB_EXTB_EHCI_P	18 25
1248		USB_85D	USB	USB_EXTB_EHCI_N	18 25
1250		USB_85D	USB	USB_EXTB_XHCI_P	18 25
1249		USB_85D	USB	USB_EXTB_XHCI_N	18 25
1227	USB3_EXT_RX	USB_85D	USB3_PCH_RX	USB3_EXTA_RX_P	18 42
1228		USB_85D	USB3_PCH_RX	USB3_EXTA_RX_N	18 42
1229	USB3_EXT_TX	USB_85D	USB3_PCH_TX	USB3_EXTA_TX_P	18 42
1230		USB_85D	USB3_PCH_TX	USB3_EXTA_TX_N	18 42
1231	USB3_EXT_RX	USB_85D	USB3_PCH_RX	USB3_EXTB_RX_P	18 43
1232		USB_85D	USB3_PCH_RX	USB3_EXTB_RX_N	18 43
1233	USB3_EXT_TX	USB_85D	USB3_PCH_TX	USB3_EXTB_TX_P	18 43
1234		USB_85D	USB3_PCH_TX	USB3_EXTB_TX_N	18 43
1235		USB_85D	USB3_PCH_RX	USB3_EXTA_RX_F_P	42
1236		USB_85D	USB3_PCH_RX	USB3_EXTA_RX_F_N	42
1237		USB_85D	USB3_PCH_TX	USB3_EXTA_TX_F_P	42
1238		USB_85D	USB3_PCH_TX	USB3_EXTA_TX_F_N	42
1240		USB_85D	USB3_PCH_RX	USB3_EXTB_RX_F_P	43
1239		USB_85D	USB3_PCH_RX	USB3_EXTB_RX_F_N	43
1241		USB_85D	USB3_PCH_TX	USB3_EXTB_TX_F_P	43
1242		USB_85D	USB3_PCH_TX	USB3_EXTB_TX_F_N	43
1243		USB_85D	USB3_PCH_TX	USB3_EXTA_TX_C_P	42
1244		USB_85D	USB3_PCH_TX	USB3_EXTA_TX_C_N	42
1245		USB_85D	USB3_PCH_TX	USB3_EXTB_TX_C_P	43
1246		USB_85D	USB3_PCH_TX	USB3_EXTB_TX_C_N	43
1251	USB_EXTA	USB_85D	USB	USB_SMC_P	8 45
1252		USB_85D	USB	USB_SMC_N	8 45
	USB_EXTC	USB_85D	USB	USB_EXTC_P	8 18
		USB_85D	USB	USB_EXTC_N	8 18
	USB_CAMERA	USB_85D	USB	USB_CAMERA_P	18 32
		USB_85D	USB	USB_CAMERA_N	18 32
	USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	6 32
		USB_85D	USB	USB_CAMERA_CONN_N	6 32
	USB_BT	USB_85D	USB	USB_BT_P	8 32
	USB_BT	USB_85D	USB	USB_BT_N	8 32
1253	USB_BT	USB_85D	USB	USB_BT_CONN_P	6 32
1254	USB_BT	USB_85D	USB	USB_BT_CONN_N	6 32
	USB_TPAD	USB_85D	USB	USB_TPAD_P	8 53
		USB_85D	USB	USB_TPAD_N	8 53
	USB_IR	USB_85D	USB	USB_IR_P	8 44
		USB_85D	USB	USB_IR_N	8 44
	PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
	PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16
	PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16
	PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16
	PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16
	PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16
	PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16
		CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16
	LPC_CLK33M	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 24

SYNC_MASTER=K90I_MLB SYNC_DATE=02/15/2011

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PCH Constraints 1

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCI-Express Signal Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_T29_TX2TX	*	=3X_DIELECTRIC	?
PCIE_T29_TX2RX	*	=4X_DIELECTRIC	?
PCIE_T29_RX2RX	*	=3x_DIELECTRIC	?
PCIE_T29_RX2TX	*	=4x_DIELECTRIC	?
PCIE_T29_2OTHER	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_T29_TX2TX	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_T29_TX2RX	TOP,BOTTOM	=5X_DIELECTRIC	?
PCIE_T29_RX2RX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_T29_RX2TX	TOP,BOTTOM	=4x_DIELECTRIC	?
PCIE_T29_2OTHER	TOP,BOTTOM	=4x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_T29_TX	*_TX	*	PCIE_T29_TX2TX
PCIE_T29_TX	*_RX	*	PCIE_T29_TX2RX
PCIE_T29_RX	*_RX	*	PCIE_T29_RX2RX
PCIE_T29_RX	*_TX	*	PCIE_T29_RX2TX
PCIE_T29_TX	*	*	PCIE_T29_2OTHER
PCIE_T29_RX	*	*	PCIE_T29_2OTHER

SOURCE: 471984_Cheif_River_MS_PDG_1.0 and the spacing rule is adjusted per SI team feedback.

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 45 47
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 45 47
LPC_RESET_L	LPC_50S	LPC	LPC_RESET_L	24
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 24
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	24 45
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 24 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 48
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 48
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 48
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SML_PCH_1_CLK	16 48
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SML_PCH_1_DATA	16 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 57
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 57
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 57
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 57
	HDA_50S	HDA	AUD_SDI_R	57
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 57
	HDA_50S	HDA	HDA_SDOUT_R	16 24
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	
SPI_CLK	SPI_50S	SPI	SPI_CLK_R	16 47
	SPI_50S	SPI	SPI_CLK	47
SPI_MOSI	SPI_50S	SPI	SPI_MOSI_R	16 47
	SPI_50S	SPI	SPI_MOSI	47
SPI_MISO	SPI_50S	SPI	SPI_MISO	16 47
SPI_CS0	SPI_50S	SPI	SPI_CS0_R_L	16 47
	SPI_50S	SPI	SPI_CS0_L	47
[1280]	SPI_50S	SPI	SPI_MLB_CLK	46 47 56
[1281]	SPI_50S	SPI	SPI_MLB_CS_L	46 47 56
[1282]	SPI_50S	SPI	SPI_MLB_MOSI	46 47 56
[1283]	SPI_50S	SPI	SPI_MLB_MISO	46 47 56
[1292]	SPI_50S	SPI	SPI_SMC_MISO	45 46
[1289]	SPI_50S	SPI	SPI_SMC_MOSI	45 46
[1284]	SPI_50S	SPI	SPI_SMC_CLK	45 46
[1290]	SPI_50S	SPI	SPI_SMC_CS_L	45 46
	PCIE_85D	PCIE_PCH_TX	PCIE_ENET_R2D_P	36
	PCIE_85D	PCIE_PCH_TX	PCIE_ENET_R2D_N	36
PCIE_ENET_R2D	PCIE_85D	PCIE_PCH_TX	PCIE_ENET_R2D_C_P	16 36
	PCIE_85D	PCIE_PCH_TX	PCIE_ENET_R2D_C_N	16 36
PCIE_ENET_D2R	PCIE_85D	PCIE_PCH_RX	PCIE_ENET_D2R_P	16 36
	PCIE_85D	PCIE_PCH_RX	PCIE_ENET_D2R_N	16 36
	PCIE_85D	PCIE_PCH_RX	PCIE_ENET_D2R_C_P	36
	PCIE_85D	PCIE_PCH_RX	PCIE_ENET_D2R_C_N	36
	PCIE_85D	PCIE_PCH_TX	PCIE_AP_R2D_P	6 32
	PCIE_85D	PCIE_PCH_TX	PCIE_AP_R2D_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE_PCH_TX	PCIE_AP_R2D_C_P	16 32
	PCIE_85D	PCIE_PCH_TX	PCIE_AP_R2D_C_N	16 32
PCIE_AP_D2R	PCIE_85D	PCIE_PCH_RX	PCIE_AP_D2R_P	16 32
	PCIE_85D	PCIE_PCH_RX	PCIE_AP_D2R_N	16 32
	PCIE_85D	PCIE_PCH_TX	PCIE_FW_R2D_P	38
	PCIE_85D	PCIE_PCH_TX	PCIE_FW_R2D_N	38
PCIE_FW_R2D	PCIE_85D	PCIE_PCH_TX	PCIE_FW_R2D_C_P	16 38
	PCIE_85D	PCIE_PCH_TX	PCIE_FW_R2D_C_N	16 38
PCIE_FW_D2R	PCIE_85D	PCIE_PCH_RX	PCIE_FW_D2R_P	16 38
	PCIE_85D	PCIE_PCH_RX	PCIE_FW_D2R_N	16 38
	PCIE_85D	PCIE_PCH_RX	PCIE_FW_D2R_C_P	38
	PCIE_85D	PCIE_PCH_RX	PCIE_FW_D2R_C_N	38
PCIE_AP_D2R	PCIE_85D	PCIE_PCH_RX	PCIE_AP_D2R_PI_P	6 32
	PCIE_85D	PCIE_PCH_RX	PCIE_AP_D2R_PI_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE_PCH_RX	PCIE_AP_R2D_PI_P	
	PCIE_85D	PCIE_PCH_RX	PCIE_AP_R2D_PI_N	
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PEG_CLK100M_N	8 16
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 36
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 36
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 32
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 38
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_P	8 16
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_EXCARD_N	8 16
[1332]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6
[1330]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6
[1317]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6
[1318]	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	
[1319]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 81
[1340]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 81
[1341]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6
[1342]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6
[1343]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6
[1344]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6
[1345]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6
[1346]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6
[1347]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	
[1348]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6
[1349]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6
[1350]	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
[1262] DP_EXTA_ML	DP_85D	DP_PCH_TX	DP_EXTA_ML_C_P<3..0>	8 75
[1263] DP_EXTA_ML	DP_85D	DP_PCH_TX	DP_EXTA_ML_C_N<3..0>	8 75
[1263]	DP_85D	DP_PCH_TX	DP_EXTA_ML_P<3..0>	75
[1263]	DP_85D	DP_PCH_TX	DP_EXTA_ML_N<3..0>	75
[1264] DP_EXTA_AUXCH	DP_85D	DP_PCH	DP_EXTA_AUXCH_C_P	8 75
[1265] DP_EXTA_AUXCH	DP_85D	DP_PCH	DP_EXTA_AUXCH_C_N	8 75
[1267]	DP_85D	DP_PCH	DP_EXTA_AUXCH_P	75
[1266]	DP_85D	DP_PCH	DP_EXTA_AUXCH_N	75
[1271] PCIE_T29_R2D	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_C_P<3..0>	8 33
[1273] PCIE_T29_R2D	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_C_N<3..0>	8 33
[1272] PCIE_T29_R2D	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_P<3..0>	33
[1274] PCIE_T29_R2D	PCIE_85D	PCIE_T29_RX	PCIE_T29_R2D_N<3..0>	33
[1270] PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_P<3..0>	8 33
[1275] PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_N<3..0>	8 33
[1277] PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_C_P<3..0>	33
[1276] PCIE_T29_D2R	PCIE_85D	PCIE_T29_TX	PCIE_T29_D2R_C_N<3..0>	33
[1278] PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 33
[1286] PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 33

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
[1281] SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 24
[1282] SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	16 24
[1283]	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	16
[1284]	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	24 36
[1285]	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R	
[1286] SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	24 33
[1287]	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	33

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

et Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
	ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
	ENET_50S	ENET_3X	ENET_RESET_L	30 36
ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	36 37
	ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	36 37
I160 CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>	
I167 CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_CMD	
I168 CR_CLK	ENET_50S	ENET_CR_DATA	ENET_CR_CLK	
I169 CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>	30 36
I170 CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_CMD	30 36
I171 CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK	30 36
I172 CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK_L	

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I159 FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_P	38 40
I158 FW_P0_TPA	FW_110D	FW_TP	FW_P0_TPA_N	38 40
I160 FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_P	38 40
I161 FW_P0_TPB	FW_110D	FW_TP	FW_P0_TPB_N	38 40
I162 FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_P	38 40
I163 FW_P1_TPA	FW_110D	FW_TP	FW_P1_TPA_N	38 40
I164 FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_P	38 40
I165 FW_P1_TPB	FW_110D	FW_TP	FW_P1_TPB_N	38 40

Port 2 Not Used

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Ethernet/FW Constraints

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29 IC Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
162		DP_85D	DP_PCH_TX	DP_T29SNK0_ML_C_P<3..0>	8 33
163		DP_85D	DP_PCH_TX	DP_T29SNK0_ML_C_N<3..0>	8 33
163	DP_T29SNK0_ML	DP_85D	DP_PCH_TX	DP_T29SNK0_ML_P<3..0>	33
164	DP_T29SNK0_ML	DP_85D	DP_PCH_TX	DP_T29SNK0_ML_N<3..0>	33
165		DP_85D	DP_PCH	DP_T29SNK0_AUXCH_C_P	8 33
166		DP_85D	DP_PCH	DP_T29SNK0_AUXCH_C_N	8 33
167	DP_T29SNK0_AUXCH	DP_85D	DP_PCH	DP_T29SNK0_AUXCH_P	33
168	DP_T29SNK0_AUXCH	DP_85D	DP_PCH	DP_T29SNK0_AUXCH_N	33
169		DP_85D	DP_PCH_TX	DP_T29SNK1_ML_C_P<3..0>	8 33
170		DP_85D	DP_PCH_TX	DP_T29SNK1_ML_C_N<3..0>	8 33
171	DP_T29SNK1_ML	DP_85D	DP_PCH_TX	DP_T29SNK1_ML_P<3..0>	33
172	DP_T29SNK1_ML	DP_85D	DP_PCH_TX	DP_T29SNK1_ML_N<3..0>	33
174		DP_85D	DP_PCH	DP_T29SNK1_AUXCH_C_P	8 33
173		DP_85D	DP_PCH	DP_T29SNK1_AUXCH_C_N	8 33
175	DP_T29SNK1_AUXCH	DP_85D	DP_PCH	DP_T29SNK1_AUXCH_P	33
176	DP_T29SNK1_AUXCH	DP_85D	DP_PCH	DP_T29SNK1_AUXCH_N	33
177		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
178		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
179		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
180		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	
181		T29_I2C_55S	T29_I2C	I2C_T29_SCL	33 48
182		T29_I2C_55S	T29_I2C	I2C_T29_SDA	33 48
183	T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	33
184	T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	33
185	T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	33
186	T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	33
187		T29DP_80D	T29DP	T29_R2D_C_P<3..0>	8 33 75
188		T29DP_80D	T29DP	T29_R2D_C_N<3..0>	8 33 75
189		T29DP_100D	T29DP	T29_D2R_P<3..0>	8 33 75
190		T29DP_100D	T29DP	T29_D2R_N<3..0>	8 33 75

Only used on hosts supporting T29 video-in

Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
1E	T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	75
1F	T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	75
1G	T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	75
1H	T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	75
1J		T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	
1K		T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	
1C	T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	75 76
1D	T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	75 76
1A	T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	75 76
1B	T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	75 76
1L1		T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	76
1L2		T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	76
1L3		T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	75
1L5		T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	75
1L4		T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	75
1L7		T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	75
1L6	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	75 83
1L8	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	75 83
1L9	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	75
1L0	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	75
1L1	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	75
1L2	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	75
1L3		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	75
1L4		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	75
1L5		T29DP_80D	T29DP	T29DPA_ML_P<3..0>	75 76
1L6		T29DP_80D	T29DP	T29DPA_ML_N<3..0>	75 76
1L7		T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	75 76
1L8		T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	75 76
1L0		T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	75 76
1L9		T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	75 76
1M1	T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
1M2	T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
1M4	T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
1M3	T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
1M5		T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>	
1M6		T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>	
1M7	T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
1M9	T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
1M8	T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
1M0	T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
1M1		T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
1M2		T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
1M3		T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
1M4		T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
1M6		T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
1M5		T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
1M7	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	83
1M8	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	83
1M9	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
1M0	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
1M1	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
1M2	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
1M3		T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
1M4		T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
1M5		T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
1M6		T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
1M7		T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
1M8		T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
1M9		T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
1M0		T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1T01_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_2_S3_SCL	6 45 48
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_2_S3_SDA	6 45 48
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_1_S0_SCL	45 48
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_1_S0_SDA	45 48
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	45 48
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	45 48
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_5_G3_SCL	6 45 48
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_5_G3_SDA	6 45 48
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_3_SCL	45 48
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_3_SDA	45 48

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1T01_DIFFPAIR		CHGR_CSI_P	64
	1T01_DIFFPAIR		CHGR_CSI_N	64
CHGR_CSO	1T01_DIFFPAIR		CHGR_CSO_P	64
	1T01_DIFFPAIR		CHGR_CSO_N	64

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SMC Constraints

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	CLK_PCIE	*	GND_P2MM
GND	PCIE*	*	GND_P2MM
GND	SATA*	*	GND_P2MM
GND	USB*	*	GND_P2MM
SB_POWER	CLK_PCIE	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM
SB_POWER	SATA*	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	LVDS*	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

J30 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	37
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	37
	SATA_90D	SATA_PCH_RX	SATA_ODD_D2R_C_P	6 41
	SATA_90D	SATA_PCH_RX	SATA_ODD_D2R_C_N	6 41
	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_RDROUT_P	41
	SATA_90D	SATA3_PCH_RX	SATA_HDD_D2R_RDROUT_N	41
	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RDRIN_P	41
	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RDRIN_N	41
1299	SATA_90D	SATA3_PCH_TX	SATA_HDD_D2R_RDRIN_P	41
1299	SATA_90D	SATA3_PCH_TX	SATA_HDD_D2R_RDRIN_N	41
1299	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RDROUT_P	41
1299	SATA_90D	SATA3_PCH_TX	SATA_HDD_R2D_RDROUT_N	41
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	THMSNS_D1_P	51
	THERM_1TO1_55S	THERM	THMSNS_D1_N	51
1287 SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	THMSNS_D2_P	51
1288	THERM_1TO1_55S	THERM	THMSNS_D2_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	51
	THERM_1TO1_55S	THERM	T29_THERMD_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29THMSNS_D2_P	
	THERM_1TO1_55S	THERM	T29THMSNS_D2_N	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	49 70
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	49 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	49 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	49 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	49 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	49 69
1315 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_P	49 69
1316	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2G_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	49
1322 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_P	49
1323	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNSG_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	49
1249 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSA50_CS_P	65
1250	SENSE_1TO1_55S	SENSE	VCCSA50_CS_N	65
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_P	
1251	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_N	68 69
1253 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPU_THERMD_P	8 9
1254	SENSE_1TO1_55S	SENSE	CPU_THERMD_N	8 9
1256 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_5V_S0_HDD_N	49
1255	SENSE_1TO1_55S	SENSE	ISNS_5V_S0_HDD_P	49
1281 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_5V_S0_HDD_R_N	49
1282	SENSE_1TO1_55S	SENSE	ISNS_5V_S0_HDD_R_P	49
1283 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
1284	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
1292 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_P	49
1291	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_N	49
1319 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_R_P	49
1320	SENSE_1TO1_55S	SENSE	ISNS_1V5_S3_DDR_R_N	49
1293	LVDS_90D	LVDS_PCH_TX	LVDS_CONN_A_CLK_F_N	6 74
1294	LVDS_90D	LVDS_PCH_TX	LVDS_CONN_A_CLK_F_P	6 74

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 32
	1TO1_DIFFPAIR		CHGR_CSI_R_P	64
	1TO1_DIFFPAIR		CHGR_CSI_R_N	64
	1TO1_DIFFPAIR		CHGR_CSO_R_P	64
	1TO1_DIFFPAIR		CHGR_CSO_R_N	64
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT	6 60 61
1298 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_N	60
1300 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_P	60
1302 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_N	60
1303 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_P	60
1304 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_N	60
1306 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_P	60
1308 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_R	57 60
1307 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_R	57 60
1309 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_N_R	57 60
1310 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_P_R	57 60
1305 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_L	57 60
1300 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_L	57 60
1314 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_P	60
1312 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_N	60
1313 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	60
1311 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	60
1315 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_P	60
1316 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_N	60
	USB_85D	USB	USB_TPAD_R_P	53
	USB_85D	USB	USB_TPAD_R_N	53
		SB_POWER	PP3V3_S5	6 7
		SB_POWER	PP3V3_S0	6 7
		SB_POWER	PP1V5_S3RS0	6 7
		GND	GND	

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Project Specific Constraints

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K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SE	ISL10	N	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	ISL3,ISL4,ISL9	Y	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.190 MM	0.1 MM			
37_OHM_SE	ISL10	N	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	ISL3,ISL4,ISL9	Y	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.235 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	ISL10	N	0.140MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.1 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.111 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.068 MM	0.068 MM		0.250 MM	0.250 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
48_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
6X_DIELECTRIC	*	0.420 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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